A Novel Passive Regenerative Snubber for the Phase-Shifted Full-Bridge Converter: Analysis, Design and Experimental Verification

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Dedication

This thesis is dedicated to my grandparents,
parents and brother for their endless love
and encouragement to follow my dreams.

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Abstract

The development of Wide Bandgap (WBG) devices has enabled power electronic converters to operate at much higher frequencies, voltages and high power. Working at a higher switching frequency minimises the size of magnetics but results in significant switching losses and electromagnetic interference (EMI) noise. Thus, it necessitates the use of soft-switching techniques to reduce these losses. Phase-Shifted Full-Bridge (PSFB) Converter is the most widely used soft-switching topology in the high-voltage and high-power, unidirectional, DC-DC conversion. The phase shift PWM control utilises the converter parasitics to achieve zero voltage switching (ZVS) turn ON. The gating technique allows the magnetic energy stored in the leakage inductance of the isolation transformer to charge and discharge the output capacitances of the inverter leg. However, the converter suffers from severe voltage overshoots across the rectifier bridge during the zero to the active state transition. The resonant circuit formed between the transformer leakage inductance and the parasitic diode capacitance of the rectifier is responsible for the high-voltage ringing.

Many passive and active snubbers are presented in the literature to mitigate the high-voltage overshoots across the diode bridge. While passive snubbers are relatively simple to implement than active snubbers, they are lossy. On the other hand, the active snubbers require additional gate driver circuitry and complex control.

The first part of the thesis proposes a novel passive regenerative snubber to overcome the mentioned drawbacks of the existing snubbers. The proposed snubber is ideally lossless with no control complexity. The work covers a detailed analysis of the PSFB operation with the proposed snubber while obtaining closed-form expressions for the converter state variables at the end of each topological stage. The study considers all the major converter parasitics, such as transformer leakage and magnetising inductances, and parasitic capacitances of the converter. Given the new snubber, the thesis also lays out a step-by-step PSFB design procedure utilising the analysis carried out in the first part of the work. The design aimed to develop a 100 kHz PSFB for an input voltage of 360-440 V in the output power range of 0.5-1.5 kW at a fixed output voltage of 48 V. The design approach focuses on the two design objectives - All inverter switches must achieve ZVS turn ON and the desired converter gain for all possible operating conditions.

A hardware prototype is built and tested. The experimental results validate the effectiveness of the snubber in reducing the voltage overshoot. Further, the analysis and design accuracy is verified using the measured state variables. The work, at last, presents the overall converter efficiency and the loss distribution among the converter components.

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Nomenclature

ΔI_o	Output current ripple
ΔV_o	Output voltage ripple
$\Delta V_s'$	Diode bridge voltage overshoot referred to primary
δ	skin depth
Δ_{Lm}	Rate of change of magnetising current
Δ_s	Total rate of change of filter current referred to primary and magnetising current
λ	Permeance
ϕ	Flux through the transformer core
ρ	Resistivity of wire
A_c	Cross section of the core
A_w	Window are
a_w	Filter inductor wire cross section
B_m	Peak flux density
$C_{a,Qeq}$	Snubber bridge charge equivalent capacitance
C_a	Snubber bridge diode capacitance
C_{cr}	Carrier wave
C_{ctrl}	Control signal
$C_{d,Qeq}$	Secondary rectifier charge equivalent capacitance
C_d	Secondary bridge diode capacitance
C_{ext}	Parasitic capacitance due to PCBs and heat sinks
C_f	Filter capacitance
C_{oss}	MOSFET output capacitance
C_p	Total primary capacitance
C_{Qeq}	Inverter bridge charge equivalent capacitance
C_s	Sec. diode bridge capacitance referred to primary
d	Applied duty ratio

D_{5-8} Secondary bridge diodes

$D_{a,d}$ Snubber bridge diodes

d_{eff} Effective duty ratio

d_i Insulation thickness

d_s Diameter of a single strand

E_i Maximum magnetic energy stored in the inductor

f Frequency of a sinusoidal current

f_{eff} Effective sinusoidal frequency for non sinusoidal currents

f_s Switching frequency

$H_a(x)$ MMF waveform for snubber transformer

h_a Winding height of snubber transformer

$H_m(x)$ MMF waveform for main transformer

h_m Winding height of main transformer

i_{ac} Current in the secondary of T_m

I_m Total magnetising current of T_m and T_a referred to primary during active mode.

i_m Total magnetising current of T_m and T_a referred to primary

I_o Output current

I_{pk} Peak output current

I_p Primary RMS current

i_p Primary Current

I_s Secondary RMS current

I_w Current flowing in the respective winding

J Current density

K_p Peak factor of the output current

K_w Window utilisation factor

L Leakage inductance of T_m

L_a Leakage inductance of snubber transformer

L_{ext} Additional inductance added in series of L_{lk}

L_f Filter inductance

L_{lk} Leakage inductance of T_m when an external series inductance is added

L_{m1} Magnetising inductance of T_m

L_{m2} Magnetising inductance of T_a

MLT Mean length turn

mu_o Permeability of free space

N Number of turns in filter inductor

n Secondary to primary turns ratio

N_{pp} Number of turns in a single winding portion of primary

N_p Primary turns

N_{ss} Number of turns in a single winding portion of primary

N_s Secondary turns

P' Power for which transformer is designed

P_{filter} Filter inductor losses

$P_{inductor}$ External inductor losses

$P_{inverter}$ Inverter bridge losses

P_o Output power

$P_{rectifier}$ losses

$P_{snubber}$ Snubber losses

P_{sw} Total power loss of a device

P_{T_m} Main transformer losses

Q_{1-4} Inverter switches

R_{cs} Case to sink thermal Resistance

$R_{g,off}$ OFF state gate resistance

$R_{g,on}$ ON state gate resistance

R_{jc} Junction to case thermal resistance

R_{load}	Load Resistance
R_{sa}	Sink to ambient thermal resistance
s_{max}	Number of strands per twist
S_T	Total number of strands per turn of winding
T_{amb}	Ambient temperature
T_a	Snubber Transformer
$t_{d,max}$	Maximum dead time
$t_{d,min}$	Minimum dead time
T_j	Junction temperature
T_m	Main Transformer
T_{sk}	Sink temperature
T_s	Switching period
v_a	Pole voltage of snubber bridge
V_{dc}	Input DC bus voltage
V_o	Output DC voltage
v_p	Pole voltage
$v_{s'}$	Voltage v_s referred to primary
v_s	Transformer secondary voltage
w_p	primary winding conductor cross-section
w_s	Secondary winding conductor cross-section

Chapter1

Introduction

1.1 Background and Motivation

Power Electronic Converters (PECs) are indispensable part of renewable energy integration, automotive industry and traction, telecom power supplies, and energy storage systems. For instance, a PEC utilises AC power to charge a battery by converting AC into DC. Moreover, this PEC controls its charging to avoid any premature battery failure. PECs are desired to be low-cost, highly efficient, smaller in size, and meet electric safety requirements.

Recent developments in Wide Band Gap (WBG) devices have influenced engineers to build even higher power-density converters at reduced costs. Thanks to their wide bandgap between the valence and the conduction band that allows high-frequency switching at higher voltages and temperatures [1].

Pushing to higher switching frequencies minimises the size of magnetics but results in higher switching losses and noise due to electromagnetic interference (EMI). Thus, there is a necessity to reduce these switching losses in PECs.

1.2 Isolated Unidirectional DC-DC Converters

In many power electronics applications, it is desired to integrate an isolation transformer into the switching converter for the following reasons [2].

- The input and output of galvanically isolated power supplies do not share a common ground, breaking the ground loops.
- Better optimisation when a large step-down or step-up conversion ratio is required.
- A converter can obtain multiple outputs by adding multiple secondary windings in the transformer.

These isolated converters can be categorised as uni- or bi-directional, depending on the direction of the power flow. The power flows from source to load in a unidirectional converter, while it flows in either direction in another. Unidirectional isolated DC-DC converters have a wide range of applications, including telecom and server power supplies, electric vehicle chargers, fuel cells, and solar PV grid integration [3].

Many isolated unidirectional converter topologies have been proposed in the literature. Converters like flyback, forward, and isolated versions of Cuk and SEPIC are used in low-voltage, and low-power applications [2, 4–6]. Traditional Pulse Width Modulated (PWM)

converters are used in high voltage and high power applications but are hard-switched and have high EMI. Essentially a PWM converter, Phase-Shifted Full-Bridge (PSFB) is an isolated version of the buck converter used in most high-power (>1 kW) applications. The PSFB allows soft-switching of the inverter switches and therefore has lesser EMI issues [7, 8]. However, the soft-switching in a PSFB is lost at low loads. Resonant-based power converters such as LLC can achieve soft-switching over the entire load range. However, LLC requires variable frequency operations making filter design and control complicated. The gain is also essentially load-dependent in resonant converters [9]. Another limitation of LLC-based converters is their ability to achieve a narrow range of converter gain. Dual-Active-Bridge based DC-DC converter achieves a wide gain range and soft-switching over a wide operating condition [10]. DAB also operates at a constant switching frequency. But both LLC and DAB incur higher conduction loss when compared with PSFB. As PSFB has a relatively simple modulation and control strategy, it is still used in most applications.

1.3 Phase-Shifted Full-Bridge

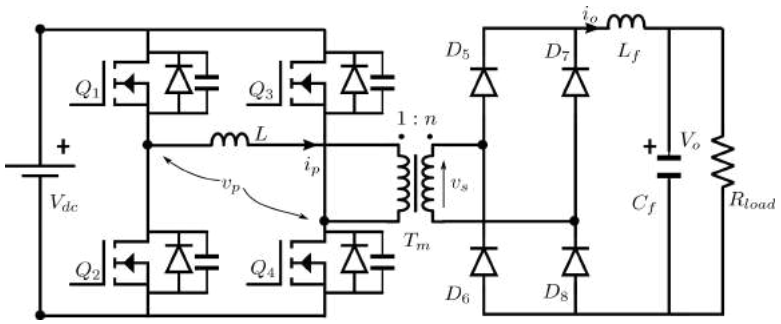


Fig. 1.1: Phase-Shifted Full-Bridge Converter

A PSFB Converter is one of the most widely used soft-switching topologies in industry applications [11, 12]. The phase-shifted PWM control scheme helps achieve Zero Voltage Switching (ZVS) of the primary bridge using circuit parasitics. The turning ON of the switches when the switch voltage is zero leads to a lossless switching known as zero voltage switching. It allows accomplishing high operating frequencies with high power densities and reduced EMI.

Fig 1.1 shows a PSFB converter consisting of an inverter bridge, a transformer T_m to provide galvanic isolation and required voltage amplification, a rectifier bridge and an output filter. Using phase-shifted PWM control, the magnetic energy stored in the inductance L charges and discharges the output capacitances of the inverter leg during the dead time between the associated gate signals of the complementary switch pair. Inductance L could be the leakage inductance L_{lk} of T_m or a series combination of L_{lk} and an additional inductor L_{ext}.

PSFB Modulation Strategy:

Consider a control signal C_{ctrl} with a 50% duty ratio of frequency $f_s/2$ and a positive slope uni-polar saw-tooth carrier wave C_{cr} of frequency f_s. Comparing C_{cr} with a modulation signal $d_m(t) = d \times V_{cr}$ generates a signal M. V_{cr} is the peak of the signal C_{cr} and d is the required duty ratio. The gating signals for the switches are thus derived as follows.

$$Q_1 = C_{ctrl}$$

$$Q_2 = \overline{Q_1}$$

$$Q_3 = C_{ctrl} \otimes M$$

$$Q_4 = \overline{Q_3}$$

The modulation strategy is shown in Fig 1.2. Thus, both legs of the bridge operate

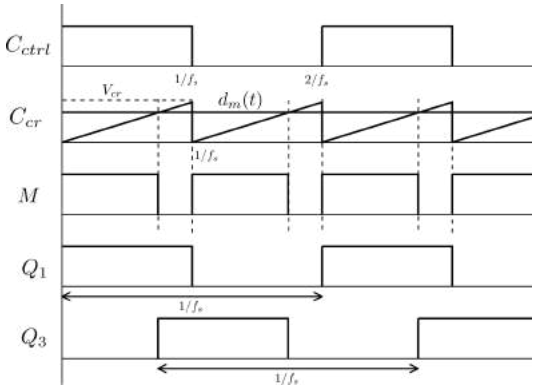


Fig. 1.2: PSFB modulation strategy

with a 50% duty. The phase between the two legs is controlled to achieve desired gain. The converter has two operational states: active and zero. The power is transferred from the source to load during active mode and freewheels in the converter during the passive mode [13]. The two legs of the inverter look symmetrical, but the phase-shift control introduces an asymmetry due to which the two legs behave differently during the switching transitions. The leg switching from active to zero state is called the leading leg, while the one switching from zero to the active state is called the lagging leg [14].

However with all the advantages of the PSFB, it suffers from a few limitations of severe voltage overshoots in the secondary, narrow ZVS range, large duty cycle loss, and conduction losses during free-wheeling [15].

1.4 The Problem of Secondary Voltage Overshoots

Consider the PSFB equivalent model shown in Fig 1.3(a). The parasitic capacitance of

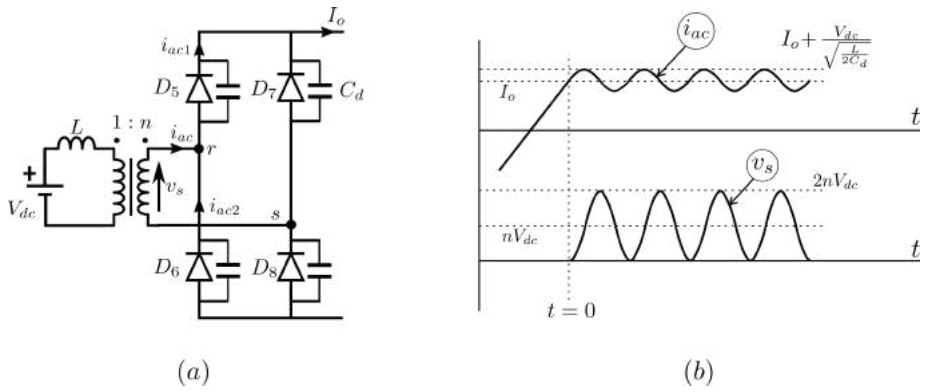


Fig. 1.3: (a) Rectifier bridge during active mode. (b) Rectifier voltage overshoot waveforms.

the diodes shown is C_d. Assume the the voltage $v_p' = +V_{dc}$ and $v_s = 0$ before $t = 0$. The current i_{ac} is $+ve$ but less than the load current I_o. The current i_{ac1} and i_{ac2} are given as follows.

$$i_{ac1} = \frac{I_o + i_{ac}}{2} \tag{1.1}$$

$$i_{ac2} = \frac{I_o - i_{ac}}{2} \tag{1.2}$$

(1.1) and (1.2) show that the two currents i_{ac1} and i_{ac2} are $+ve$ therefore, all diodes of the rectifier are in conduction. The current i_{ac} rises linearly at a rate of V_{dc}/nL A s^{-1}. As i_{ac} reaches I_o, $i_{ac1} = I_o$ and $i_{ac2} = 0$, diodes D_6 and D_7 stop conducting and get reverse biased. As i_{ac} increases further and the i_{a2} becomes negative, diode capacitances of D_6 and D_7 show up to form a resonant circuit with n^2L. Solving the equivalent circuit gives

$$n^2 L \frac{di_{ac}(t)}{dt} = nV_{dc} - v_s$$

$$2C_d \frac{dv_s(t)}{dt} = i_{ac} - I_o$$

Using the above equations, we get

$$2n^2 LC_d \frac{d^2 v_s(t)}{dt^2} = nV_{dc} - v_s \tag{1.3}$$

Solving the differential equation (1.3), v_s and i_{ac} can be expressed as

$$v_s(t) = nV_{dc}\left\{1 - \cos\left(\frac{1}{\sqrt{2n^2 LC_d}}t\right)\right\} \tag{1.4}$$

$$i_{ac}(t) = \frac{V_{dc}}{\sqrt{\frac{L}{2C_d}}} \sin\left(\frac{1}{\sqrt{2n^2 LC_d}}t\right) \tag{1.5}$$

Equation (1.4) and Fig 1.3(b) show that the rectifier voltage overshoots can go up to twice the secondary referred DC bus voltage V_{dc}. Thus, it increases the voltage rating of rectifier diodes and makes them susceptible to overvoltage breakdown.

1.5 Existing Snubber Solutions

Several remedies (snubbers) have been proposed in the literature to mitigate the secondary bridge voltage overshoots. These snubbers can broadly be classified as shown in Fig 1.4. Fig 1.5 shows a PSFB converter with some widely used snubber circuits. L_{lk} is the leakage

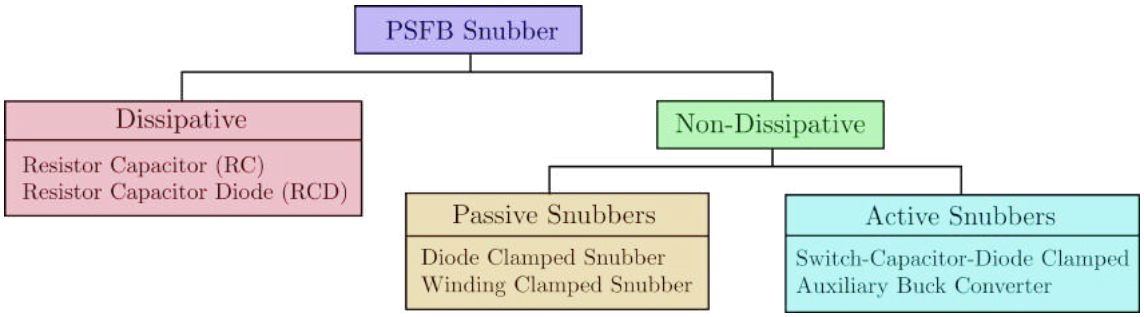


Fig. 1.4: Classification of snubbers for Phase-Shifted Full-Bridge

inductance of the transformer T_m, and L_{ext} represents the externally added inductor and can be zero or have a finite value.
The following section briefly discusses some popular snubber topologies and their respective advantages and limitations. Active snubbers are usually a combination of passive elements like capacitance, inductance and diodes with an active element, i.e. a switch.

Resistor-Capacitor (RC)

The traditional RC circuit across the rectifier diodes can dampen the voltage overshoots across the rectifier bridge. However, the total excess energy is lost in the damping resistor.

Resistor-Capacitor-Diode (RCD)

An alternative solution can be a RCD snubber [16]. The RCD clamped snubber is composed of C_{snb}, D_{snb}, and R_{snb}, as shown in Fig 1.5(b). C_{snb} is large enough to be assumed as a constant voltage source V_c. As v_s reaches V_c, D_{snb} gets forward biased, clamping v_s at V_c. The excess current flows through the snubber capacitance C_{snb}. Resistance R_{snb} provides the discharge path for the charge balance of C_{snb}. A portion of this energy gets transferred to the load, and the rest is lost in R_{snb}.
The advantage of using an RCD snubber is its simple design and no requirement of additional circuitry. However, this too turns out to be an inefficient solution for high-voltage and high-power converters.

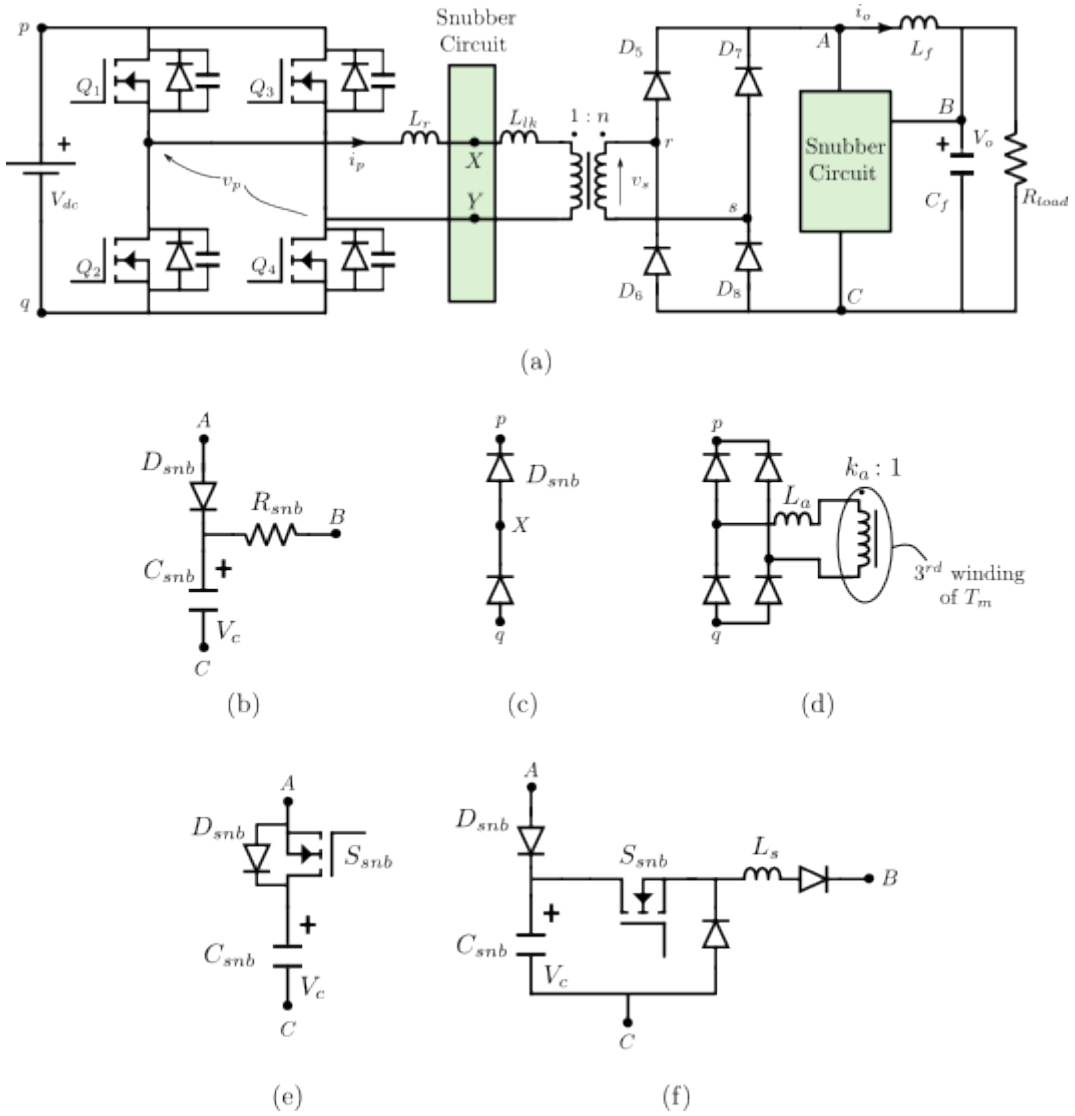


Fig. 1.5: PSFB converter with some popular snubber topologies. (a) Highlighted snubber positions. (b) RCD (c) Diode-Clamped Snubber (d) Winding-Clamped (e) Switch-Diode-Clamped (f) Auxiliary Buck Converter

Switch-Diode-Clamped

A non-dissipative Switch-Capacitor-Diode Clamped snubber 1.5(e) proposed in [17] replaces the resistive path of the RCD snubber with a switch S_{snb} to discharge C_{snb}. As voltage v_s reaches V_c, D_{snb} gets forward biased, and the excess current flows through the clamping capacitor. This extra charge stored in C_{snb} is transferred to the load by turning

ON the snubber switch S_{snb} as shown in [17] and [18].

Auxiliary Buck Converter (Non-Dissipative, Active Snubber)

The proposed Auxiliary Buck Converter snubber circuits in [19–21] clamp the secondary voltage v_s to V_c through D_{snb} and C_{snb}, similar to switch-capacitor-clamped snubber. The difference lies in the clamping capacitor discharging strategy. These solutions propose an auxiliary buck converter operating in discontinuous and boundary conduction mode to create a path for charge balancing of C_{snb} as shown in Fig 1.5(f).

The active snubbers effectively clamp the diode bridge voltage overshoots to a clamping voltage V_c. These lossless and regenerative snubbers are efficacious in clamping the oscillations due to both L_{ext} and L_{lk}. However, they suffer from the following drawbacks.

- A complex control scheme for clamping capacitor charge balancing.
- An auxiliary gate driver circuitry increases the component count and decreases system reliability.
- The switch S_{snb} in many of these snubbers is hard-switched, leading to switching loss in the snubber. Although [17, 18] shows a strategy to ZVS turn ON S_{snb}, but with a complex control scheme.

Diode-Clamped Snubber

Transformer leakage L_{lk} (primary winding + secondary winding) and an external inductor L_{ext} to achieve ZVS. To reduce the inductor losses, L_{ext} is either put in the primary or the secondary, whichever has the lower current.

A diode-clamped solution is proposed in [14] that uses a resonant inductor L_{ext} and clamping diodes D_{snb}, keeping the transformer leakage inductance as low as possible. The clamping diodes fix the common point X of L_{ext} and the transformer terminal to the input DC bus, as shown in Fig 1.5(c). The other terminals of T_m and L_{ext} are connected to the lagging and leading leg, respectively.

Some significant advantages of this non-dissipative snubber are its design simplicity and low component count. However, it suffers from the following limitations.

- D_{snb} conducts twice in half the switching cycle, i.e. during the active and the passive states, increasing the conduction and switching losses in the diodes. However, its conduction is unnecessary during the zero states as the clamping action is only required during the active mode.
- It increases the current flowing through the resonant inductor L_{ext} during the freewheeling interval, causing additional conduction loss.
- It only clamps oscillations due to L_{ext} but oscillations caused by L_{lk} remain. Therefore, it necessitates to add L_{ext} and minimising the leakage inductance L_{lk}. Thus,

restricting the inductance necessary for soft-switching to be integrated into the transformer.

The **Improved Diode-Clamped** solution in [22] proposes two clamping diodes D_{snb} connected to a common point X. However, the lagging and leading legs are interchanged, so T_m and L_{ext} are connected to the leading and lagging legs, respectively.

With this simple modification, D_{snb} conducts only once in half the switching cycle, i.e. during the active state. A lower current than [14] flows through L_{ext} during the zero state. Thus, improving the overall efficiency of the converter. However, the problem of the necessity of resonant inductor and the voltage overshoot due to L_{lk} remains.

Winding-Clamped Snubber

The winding clamped snubber in [23, 24] consists of an integrated tertiary winding and a resonant capacitor C_{rr} parallel to the third winding as shown in Fig 1.5(c). The primary to tertiary winding ratio is $N_1/N_3 = k_a$. The additional winding clamps the secondary transformer voltage to nk_aaV_{dc} through a diode bridge rectifier during the active mode. Unlike the diode-clamped snubber, the snubber bridge diodes conduct only once every half switching cycle. This snubber takes care of the ringing due to the primary winding's leakage inductance. However, the secondary winding leakage inductance still rings with the parasitic capacitance of the diode bridge.

The non-dissipative passive snubbers discussed in this section do not reduce the ringing due to all the inductances L_{lk} (primary and secondary) and L_{ext}. Thus, the problem remains either due to a necessity for L_{ext} or in applications of higher load voltages.

1.6 Contribution of the Thesis

The previous sections discussed the issue of rectifier bridge voltage overshoot in a PSFB converter and some popular remedies proposed in the literature. The thesis presents a novel snubber to overcome the limitations of these solutions and design a PSFB converter and the proposed snubber for a given specification.

1.6.1 The Proposed Snubber

A PSFB snubber is desired to have the following features.

- It should effectively reduce/clamp the diode bridge voltage overshoots.
- It should be non-dissipative and regenerative.
- It must have minimum to zero active switches to improve the reliability of the snubber and add minimum auxiliary components.
- Should not have complex control such as what is required for charge balancing of clamping capacitor.

- It should provide an option to integrate the resonant inductor in the transformer.

With these features in mind, this thesis proposes a novel passive regenerative snubber. The topology comprises a snubber transformer T_a and a snubber diode bridge which clamps the secondary of the power/main transformer T_m to the DC bus voltage through T_a.

1.6.2 PSFB Design

The manuscript presents a detailed discussion of the converter operation with the novel snubber. The circuit analysis considers and models all the major parasitics like junction capacitances, leakage and magnetising inductances.

It then lays down a detailed design procedure for a phase-shifted full-bridge converter and the proposed snubber with a wide range of operating conditions considering line (input voltage) and load regulation. The design ensures the converter gain and ZVS turn-on of the switches in each operating condition. The converter operation is validated experimentally on a hardware prototype of a $360\,\mathrm{V} - 440\,\mathrm{V}/48\,\mathrm{V}$ and $1.5\,\mathrm{kW}$ step-down PSFB converter.

1.7 Organisation of the Thesis

A brief chapter-wise summary is presented as follows.

Chapter 2: Phase-Shifted Full-Bridge Analysis provides a comprehensive circuit analysis of the PSFB converter with the proposed snubber. The study obtains closed-form expressions for the converter state variables considering all the dominant circuit parasitics.

Chapter 3: Phase-Shifted Full-Bridge Design presents a detailed design procedure of the converter for the given specifications. The converter gain expression obtained in Chapter 2 is utilised to determine the transformer turns ratio and required leakage inductance to achieve ZVS turn-ON.

Chapter 4: Hardware Design discusses the design of magnetics and components selection.

Chapter 5: Experimental Verification The snubber topology and converter design are validated on a hardware prototype of $360\,\mathrm{V} - 440\,\mathrm{V}/48\,\mathrm{V}$ and $0.5 - 1.5\,\mathrm{kW}$. The final section of the chapter presents the loss distribution and overall efficiency calculations.

Chapter 6: Conclusions and future work This chapter summarizes the overall contribution of the work presented in this thesis. An outline of the future work is also given.

Chapter2

Phase-Shifted Full-Bridge Analysis

2.1 Introduction

In Chapter 1, we discussed the motivation and focus of the thesis. The simplicity of PSFB operation makes it a popular topology in medium to high voltage and power applications. However, the diode bridge voltage overshoots remain one of the major drawbacks of the converter. We discussed various solutions available in the literature and their limitations. Chapter 1 then proposes a novel passive regenerative snubber topology to overcome some of the constraints posed by the existing snubbers.
This chapter covers a detailed analysis of the PSFB converter and the proposed snubber considering all the dominant parasitics like the transformer's leakage inductances and junction capacitance of the diodes. The converter operation can be divided into eight topological stages. These eight operation modes are analysed by solving their specific equivalent circuits and deriving closed-form expressions for the state variables during the modes. The conditions required for a successful zero voltage switching are derived.

The obtained closed-form expressions in each mode are then used to determine the converter gain. This expression will help design the PSFB in Chapter 3. The chapter also presents a detailed discussion on deviations from the idealities assumed during the analysis.

2.2 Operational Analysis

Fig 2.1 shows the PSFB converter with the proposed snubber. C_{oss}, C_d, and C_a are the output and junction capacitances of the MOSFETs, secondary, and snubber diodes, respectively. Inductances L and L_a are the leakage inductances of the main transformer T_m

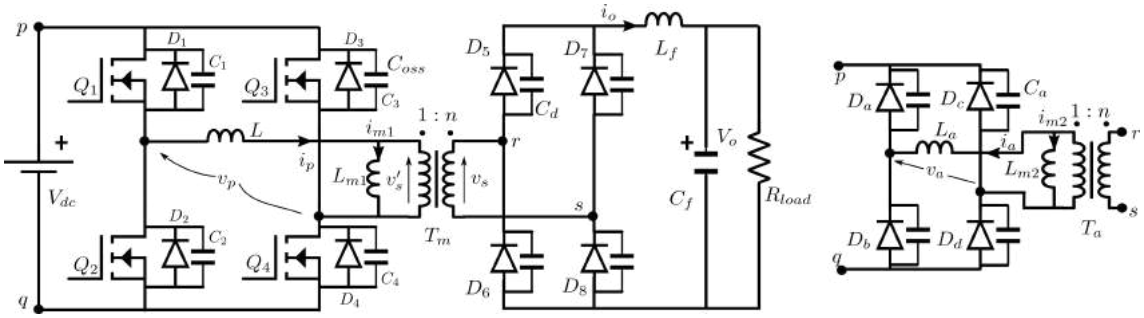


Fig. 2.1: PSFB converter with the proposed snubber.

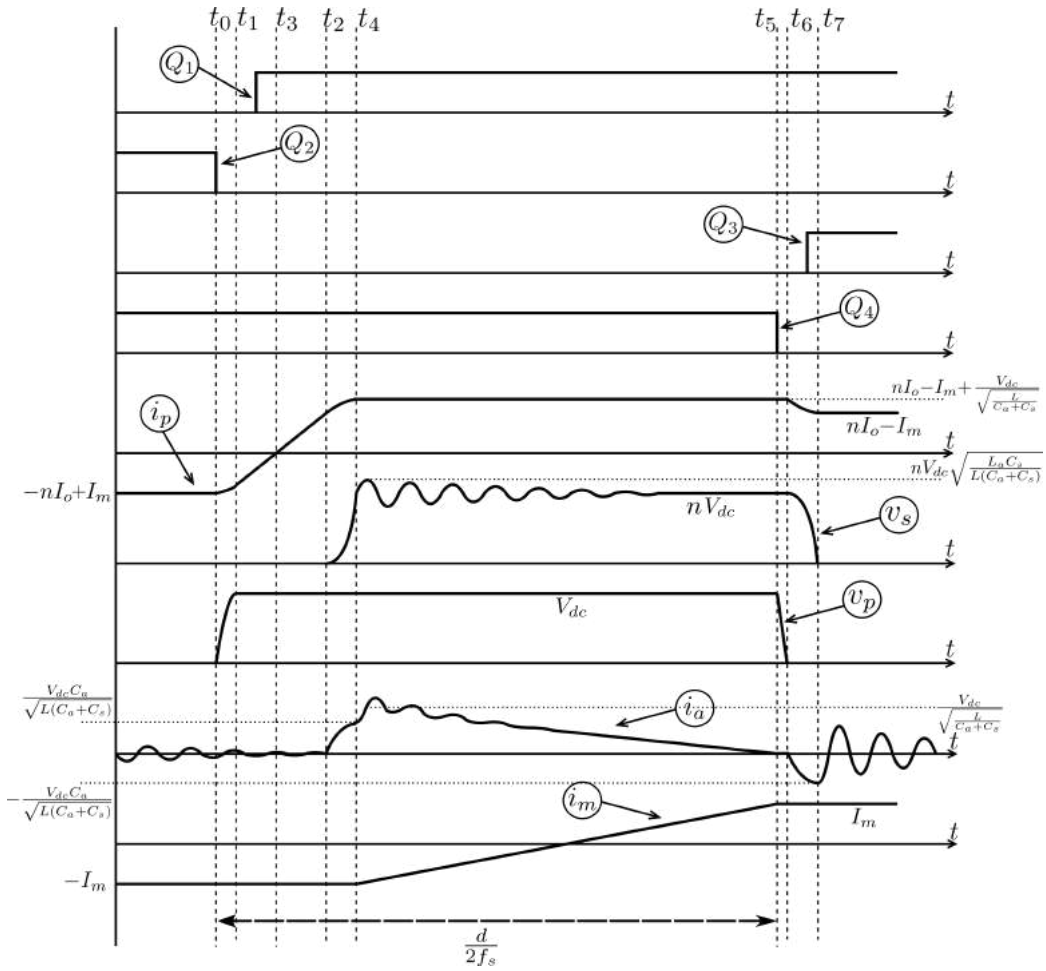


Fig. 2.2: Converter waveforms for a half-switching cycle.

and the snubber transformer T_a, respectively. The pole voltage is v_p while v_s' is the transformer's secondary voltage referred to primary. During inverter leg switching, the two output capacitances of the high and low side devices simultaneously charge to and discharge from V_{dc}. It brings the two capacitances essentially in parallel to become $C_p = 2C_{oss}$. The primary referred diode bridge's parasitic capacitance is given by $C_s = n^2 2C_d$, where n represents the secondary to the primary turns ratio of the two transformers. The effective capacitance across the AC link of the snubber bridge is C_a. The output current i_o can be assumed constant at I_o, considering a large filter inductance such that $L_f \gg L$. L_{m1} and L_{m2} are the magnetising inductances of T_m and T_a, respectively. L_m gives the parallel combination of the two magnetising inductances and the current i_m is the sum of the two magnetising currents, i_{m1} and i_{m2}. The total magnetising current i_m is approximated as a current sink with current as shown in Fig 2.2.

The PSFB converter operation is symmetrical over half the switching period T_s and can be summarised in eight topological stages. Fig 2.2 shows the state variables of the converter during these eight stages. The applied duty ratio d is defined as the ratio of the time interval between the switching of the two legs to half the switching period $T_s/2$.
To start with the analysis, let's assume that the converter is in the zero state. Switches Q_2 and Q_4 are in conduction such that $v_p = 0$.

$$v_s'(t) = 0$$

$$i_p(t) = -nI_o + I_m$$

$$i_a(t) \approx 0$$

Where t_{0^-} is the instant the zero state starts and I_m is the sum of the magnetising currents in the passive state. The above-expressed currents, can be established at the end of mode 7, i.e. at the beginning of the next zero state.

2.2.1 Mode 1 (Lagging Leg Switching)

This mode starts with the turning OFF of switch Q_2. However, the pole voltage cannot

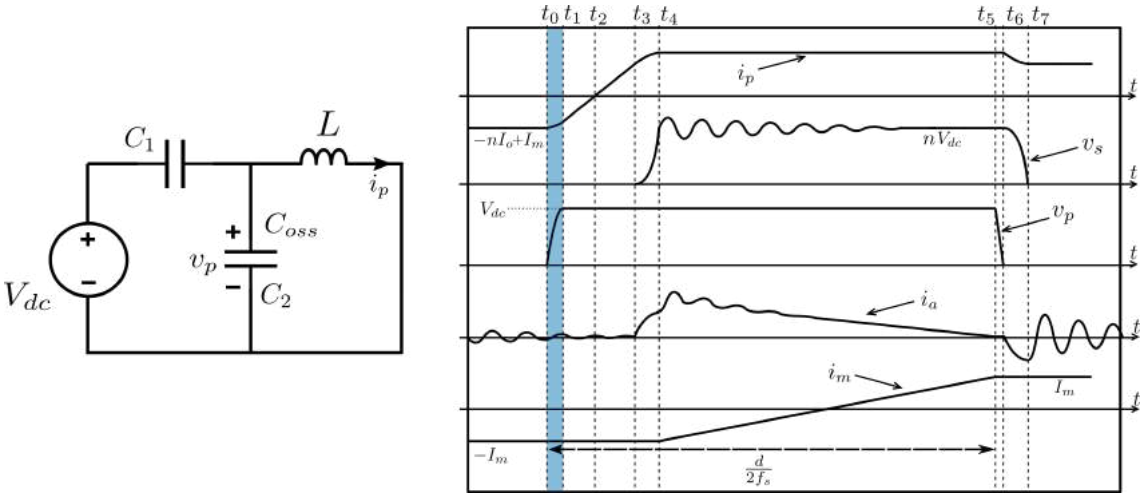


Fig. 2.3: Equivalent circuit for Mode 1

change suddenly due to the voltage-stiff element across the switches. C_2 and C_1 start to charge and discharge, respectively, as shown in the equivalent circuit in Fig 2.3. The initial conditions for the equivalent circuit are $v_p(t_0) = 0$, $i_p(t_0) = -nI_o + I_m$, and $v_s'(t_0) = 0$. Using KVL and KCL,

$$i_p(t) = -(C_1 + C_2)\frac{dv_p(t)}{dt} \tag{2.1}$$

$$v_p(t) = L\frac{di_p(t)}{dt} \tag{2.2}$$

$$i_a(t) = -C_a L_a \frac{d^2 i_a(t)}{dt^2} \tag{2.3}$$

Using (2.1) and (2.2), we get

$$i_p(t) = -(C_1 + C_2) L \frac{d^2 i_p(t)}{dt^2} \tag{2.4}$$

Where $C_1 + C_2 = 2C_{oss} = C_p$, the primary current $i_p(t)$ after solving (2.4) is given by

$$i_p(t) = -(nI_o - I_m) \cos\left(\frac{1}{\sqrt{LC_p}}(t - t_0)\right) \tag{2.5}$$

Then,

$$v_p(t) = (nI_o - I_m)\sqrt{\frac{L}{C_p}} \sin\left(\frac{1}{\sqrt{LC_p}}(t - t_0)\right) \tag{2.6}$$

$$i_a(t) \approx 0$$

The time for i_p to reach zero and v_p to reach V_{dc} are given as $t_{i_p(0)}$ and $t_{v_p(V_{dc})}$. Where

$$t_{i_p(0)} = \frac{\pi}{2}\sqrt{LC_p}$$

$$t_{v_p(V_{dc})} = \sqrt{LC_p} \sin^{-1}\left(\frac{V_{dc}\sqrt{C_p}}{(nI_o - I_m)\sqrt{L}}\right)$$

A necessary condition for ZVS turn ON is $t_{i_p(0)} \geq t_{v_p(V_{dc})}$, which gives the minimum leakage inductance L required to achieve soft switching for a given load and applied voltage.

$$L \geq C_p \left(\frac{V_{dc}}{nI_o - I_m}\right)^2 \tag{2.7}$$

Neglecting I_m w.r.t. nI_o, we get

$$L \geq C_p \left(\frac{V_{dc}}{nI_o}\right)^2 \tag{2.8}$$

If (2.7) is satisfied, the mode ends with D_2 getting reverse biased and the pole voltage getting clamped to V_{dc}. The time taken for the transition to complete is

$$t_I = t_1 - t_0 = \sqrt{LC_p} \sin^{-1}\left(\frac{V_{dc}\sqrt{C_p}}{(nI_o - I_m)\sqrt{L}}\right) \tag{2.9}$$

$$i_p(t_1) = -\left[(nI_o - I_m)^2 - \left(\frac{V_{dc}\sqrt{C_p}}{\sqrt{L}}\right)^2\right]^{1/2} \tag{2.10}$$

2.2.2 Mode 2 (Current Commutation - I)

As soon as v_p reaches V_{dc}, D_2 becomes reverse-biased, and D_1 comes into conduction. At the beginning of mode 2, $v_p(t_1) = V_{dc}$, $v_s'(t_1) = 0$, and the primary current $i_p(t_1)$ is as given in (2.10). Fig 2.4 shows the equivalent circuit for the transition. The main transformer's primary current linearly rises from $i_p(t_1)$ to zero. On secondary, On secondary, the current through D_6 and D_7 linearly decreases and transfers to diodes D_5 and D_8.
Thus, during the transition $v_s'(t) = 0$ and $v_p(t) = V_{dc}$. Solving the the equivalent circuit in Fig 2.4,

$$\begin{aligned} i_p(t) &= i_p(t_1) + \frac{1}{L}\int v_p(t)dt \\ &= i_p(t_1) + \frac{1}{L}\int V_{dc}dt \end{aligned}$$

The above equations give $i_p(t)$ as expressed in (2.11). Snubber current $i_a(t)$ remains

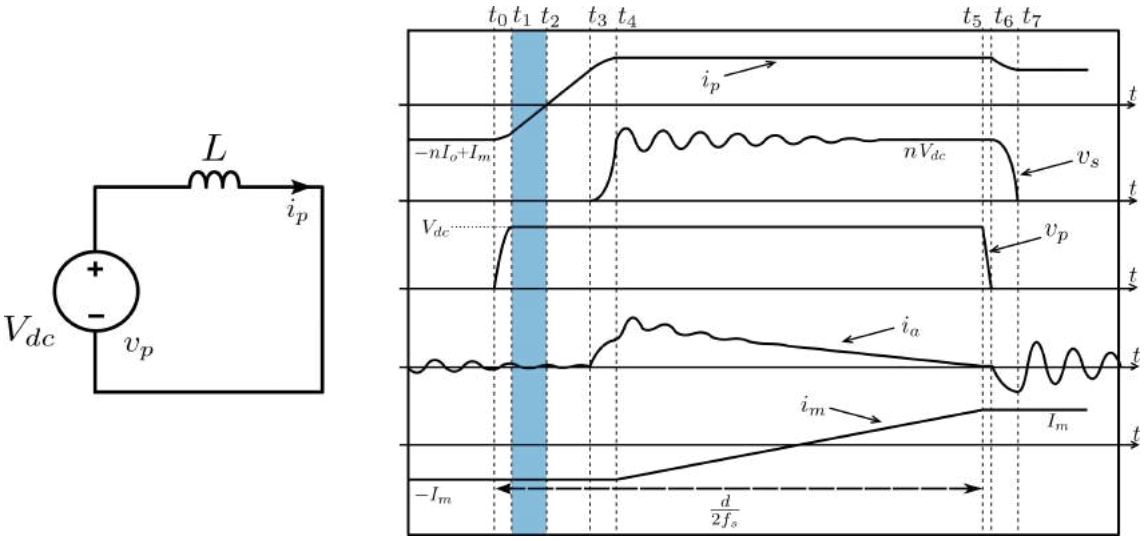


Fig. 2.4: Equivalent circuit for Mode 2

oscillating about zero as in the previous modes.

$$i_p(t) = i_p(t_1) + \frac{V_{dc}}{L}(t - t_1) \tag{2.11}$$

$$i_a(t) \approx 0$$

Time taken for i_p to reach zero is given as follows:

$$\begin{aligned} t_{II} = t_2 - t_1 &= \frac{-i_p(t_1)L}{V_{dc}} \\ &= \left[\left(\frac{(nI_o - I_m)L}{V_{dc}}\right)^2 - LC_p\right]^{1/2} \end{aligned} \tag{2.12}$$

Q_1 must be switched ON during this interval to achieve ZVS turn ON. **Therefore, the dead time requirement is,**

$$t_1 < t_{dead} < t_2$$

$$\sqrt{LC_p}\sin^{-1}\left(\frac{V_{dc}\sqrt{C_p}}{(nI_o - I_m)\sqrt{L}}\right) < t_d < \sqrt{LC_p}\sin^{-1}\left(\frac{V_{dc}\sqrt{C_p}}{(nI_o - I_m)\sqrt{L}}\right) + \left[\left(\frac{(nI_o - I_m)L}{V_{dc}}\right)^2 - LC_p\right]^{1/2} \tag{2.13}$$

2.2.3 Mode 3 (Current Commutation - II)

Device Q_1 is switched ON during Mode 2. Therefore, once the i_p crosses zero, switches Q_1 and Q_4 come into conduction. The equivalent circuit for the transition with initial

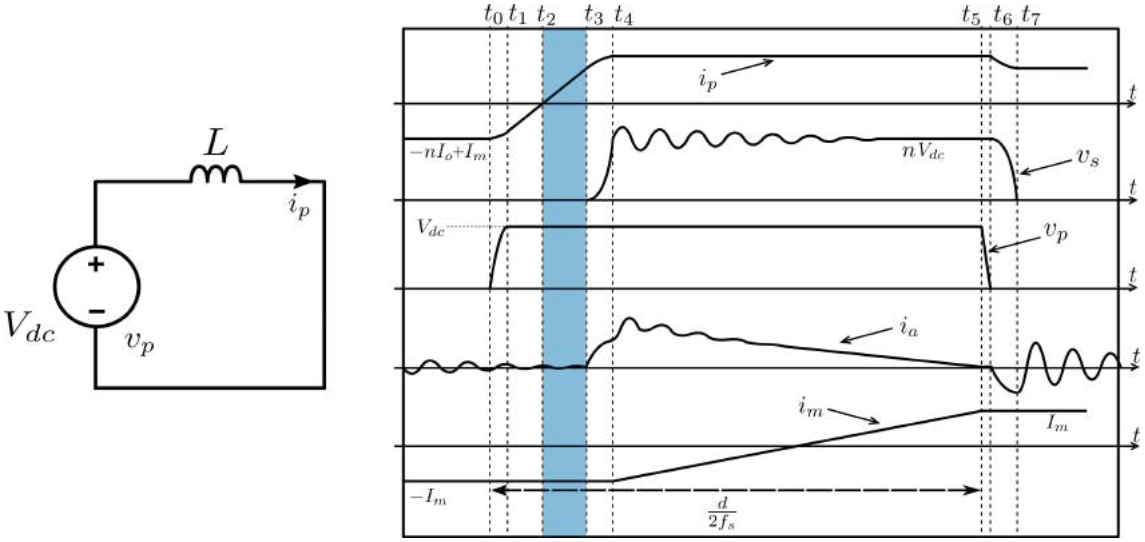


Fig. 2.5: Equivalent circuit for Mode 3

conditions as $i_p(t_2) = 0$, $v_p(t_2) = V_{dc}$, and $v_s'(t_2) = 0$ is shown in Fig 2.5. Solving for i_p, we get

$$\begin{aligned} i_p(t) &= \frac{1}{L}\int v_p(t)dt \\ &= \frac{1}{L}\int V_{dc}dt \end{aligned}$$

$$\begin{aligned} i_p(t) &= \frac{V_{dc}}{L}(t - t_2) \\ i_a(t) &\approx 0 \end{aligned} \tag{2.14}$$

The mode ends with i_p reaching the reflected output current $nI_o - I_m$ and off-diagonal diodes D_6 and D_7 going out of conduction. Time taken for the transition to end is as follows.

$$t_{III} = t_3 - t_2 = \frac{(nI_o - I_m)L}{V_{dc}} \tag{2.15}$$

Thus, by the end of this mode $i_p(t_4) = nI_o - I_m$ and $i_a(t_4) = 0$.

2.2.4 Mode 4 (Secondary Voltage Rise)

The state variables at the beginning of this mode are $i_p(t_3) = nI_o - I_m$, $i_a(t_3) = 0$, $v_p(t_3) = V_{dc}$, $v_s'(t_3) = 0$, $v_a(t_3) = 0$. It is assumed that the change in the magnetising current is negligible, and thus during mode 4, $i_m = -I_m$. The additional current charges

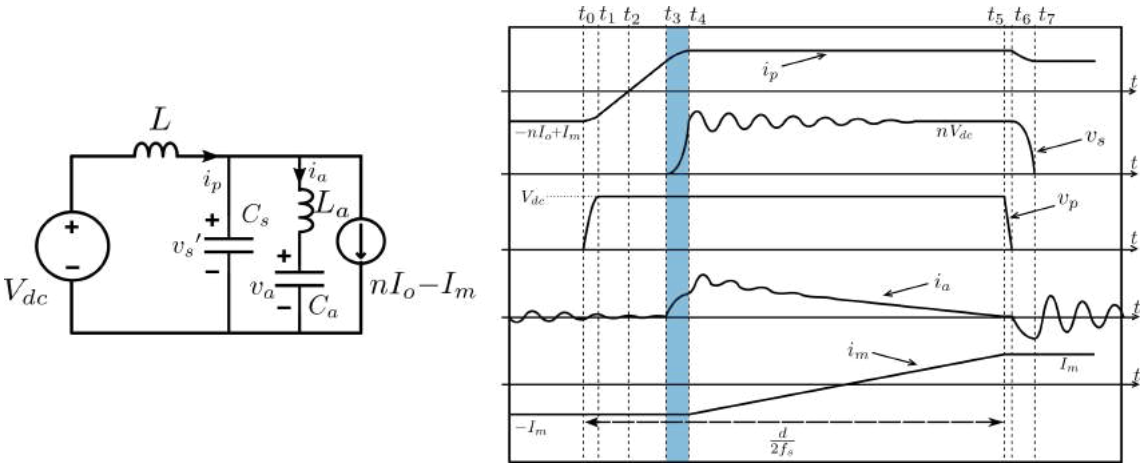


Fig. 2.6: Equivalent circuit for mode 4

the secondary and snubber capacitances as the primary current increases further $nI_o - I_m$. Fig 2.6 shows the fourth-order resonant circuit formed during this mode. Since $L \gg L_a$,

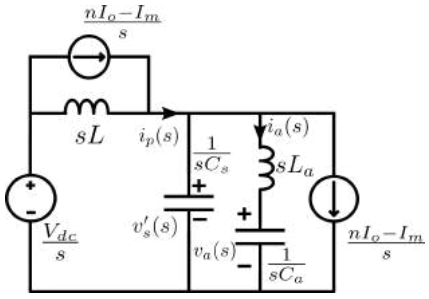


Fig. 2.7: Laplace transformed equivalent circuit for mode 4.

the fourth-order circuit can be reduced to a second-order one by roots approximation as shown by solving the Laplace transformed equivalent circuit in Fig 2.7. Using voltage

division rule, the secondary voltage $v_s'(s)$ can be expressed as in (2.16).

$$v_s'(s) = \frac{Z(s)V_{dc}}{s(Z(s)+sL)} \tag{2.16}$$

Where $Z(s) = \frac{1}{sC_s} || \left(\frac{1}{sC_a} + sL_a\right)$. Using $L \gg L_a$ we get

$$v_s'(s) = \frac{V_{dc}(s^2L_aC_a+1)}{s[s^4LL_aC_aC_s + s^2L(C_a+C_s)+1]} \tag{2.17}$$

Since $L_a\frac{C_aC_s}{C_a+C_s} \ll L(C_a+C_s)$, the denominator polynomial can be expressed as in (2.18).

$$\begin{aligned} v_s'(s) &\approx \frac{V_{dc}(s^2L_aC_a+1)}{s\left(s^2L_a\frac{C_aC_s}{C_a+C_s}+1\right)(s^2L(C_a+C_s)+1)} \\ &\approx \frac{V_{dc}(s^2L_aC_a+1)}{s(s^2L(C_a+C_s)+1)} \\ &\approx \frac{V_{dc}}{s} - \frac{sV_{dc}}{s^2+\frac{1}{L(C_a+C_s)}} \end{aligned} \tag{2.18}$$

Thus, using (2.19) $v_a(s)$ can be expressed as

$$v_a(s) = \frac{v_s'(s)}{(s^2L_aC_a+1)} \tag{2.19}$$

Equating (2.18) in (2.19) and further approximating the roots gives

$$v_a(s) \approx \frac{V_{dc}}{s} - \frac{sV_{dc}}{s^2+\frac{1}{L(C_a+C_s)}} \tag{2.20}$$

Therefore taking inverse Laplace transform of (2.18) and (2.20), we get

$$v_s{}'(t) \approx v_a(t) \approx V_{dc}\left\{1-\cos\left(\frac{1}{\sqrt{L(C_a+C_s)}}(t-t_3)\right)\right\} \tag{2.21}$$

Current flowing through L_a and L can be calculated as follows:

$$\begin{aligned} i_a(t) &= C_a\frac{dv_a(t)}{dt} \\ &\approx \frac{V_{dc}C_a}{\sqrt{L(C_a+C_s)}}\sin\left(\frac{1}{\sqrt{L(C_a+C_s)}}(t-t_3)\right) \end{aligned} \tag{2.22}$$

$$\begin{aligned} i_p(t) &= nI_o - I_m + i_a(t) + C_s\frac{dv_s(t)}{dt} \\ &\approx nI_o - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{(C_a+C_s)}}}\sin\left(\frac{1}{\sqrt{L(C_a+C_s)}}(t-t_3)\right) \end{aligned} \tag{2.23}$$

As v_a reaches V_{dc}, diodes D_b and D_c get clamped to V_{dc} while D_a and D_d start to conduct. The time taken for this mode to end is expressed as in (2.24).

$$t_{IV} = t_4 - t_3 \approx \frac{\pi}{2}\sqrt{L(C_a + C_s)} \tag{2.24}$$

$$i_p(t_4) \approx nI_o - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{(C_a+C_s)}}}$$

$$i_a(t_4) \approx \frac{V_{dc}C_a}{\sqrt{L(C_a + C_s)}}$$

$$v_s'(t_4) \approx v_a(t_4) = V_{dc}$$

2.2.5 Mode 5 (Active State)

Fig 2.8 shows the equivalent circuit for the active state. The initial conditions of the state variables during this mode are $i_p(t_4) \approx nI_o - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{(C_a+C_s)}}}$, $i_a(t_4) \approx \frac{V_{dc}C_a}{\sqrt{L(C_a+C_s)}}$, and $v_s(t_4) \approx V_{dc}$. The source transfers power to the load during this interval. The magnetising

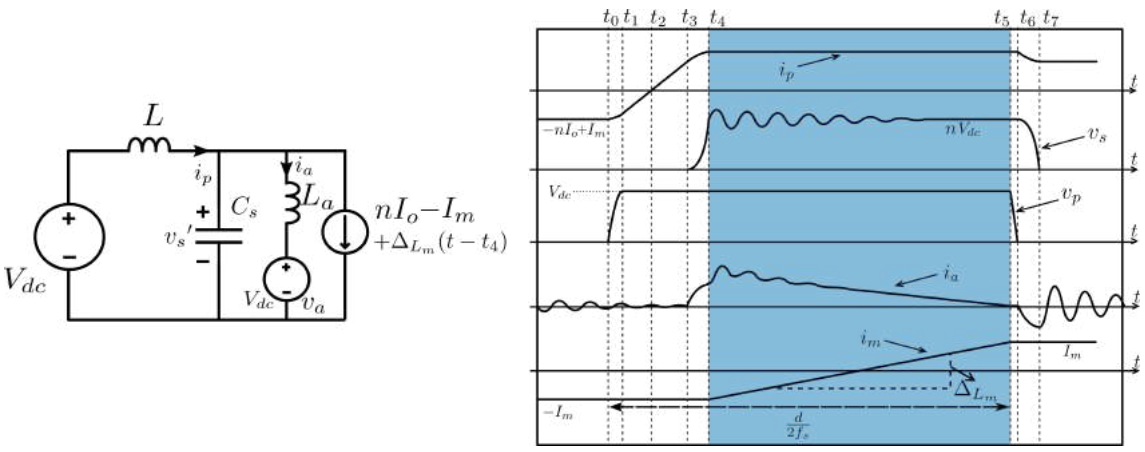


Fig. 2.8: Equivalent circuit for Mode 5.

current increases with a slope of $\Delta_{L_m} = V_{dc}/L_m$, where L_m is the parallel combination of the magnetising inductance of the main and the snubber transformer.

$$i_m(t) = -I_m + \Delta_{L_m}(t - t_4) \tag{2.25}$$

Thus, the sum of the load current and the magnetising inductance can be represented by a current ramp sink as follows.

$$i_t(t) = nI_o - I_m + \Delta_{L_m}(t - t_4) \tag{2.26}$$

The closed-form expressions of the state variables are obtained by solving the equivalent circuit using Laplace transformation as shown in Fig 2.9. Let $I_1 = nI_o - I_m$, $I_2 = \frac{V_{dc}}{\sqrt{\frac{L}{(C_a+C_s)}}}$, and $I_3 = \frac{V_{dc}C_a}{\sqrt{L(C_a+C_s)}}$. Then the Kirchoff's laws give the following equations.

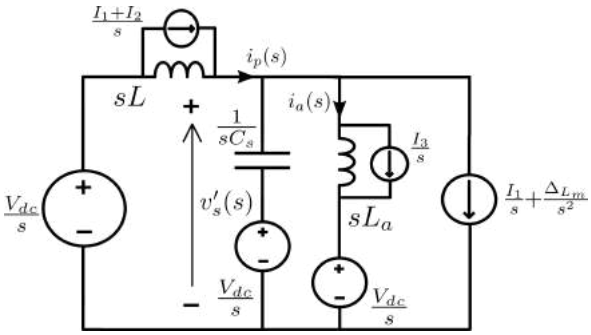


Fig. 2.9: Laplace transformed equivalent circuit for Mode 5.

$$i_p(s) = \frac{(I_1 + I_2)L + \left(\frac{I_1+I_3}{s} + \frac{\Delta_{L_m}}{s^2}\right) Z_2(s)}{sL + Z_2(s)} \tag{2.27}$$

Where $Z_2(s) = \frac{sL_a}{s^2L_aC_s+1}$. Substituting $Z_2(s)$ in (2.27) and applying $L >> L_a$, we get

$$i_p(s) \approx \frac{I_1 + I_2}{s} + \frac{L_a}{L}\left\{\frac{\Delta_{L_m}}{s^2} - \frac{\Delta_{L_m}}{\left(s^2 + \frac{1}{L_aC_s}\right)} + \frac{(I_3 - I_2)}{s} - \frac{(I_3 - I_2)s}{\left(s^2 + \frac{1}{L_aC_s}\right)}\right\} \tag{2.28}$$

Since $L >> L_a$,

$$i_p(s) \approx \frac{I_1 + I_2}{s} \tag{2.29}$$

Solving for $i_a(s)$

$$i_a(s) = \frac{I_3}{s} + \left(i_p(s) - \frac{I_1 + I_3}{s} - \frac{\Delta_{L_m}}{s^2}\right)\frac{1}{(1 + s^2L_aC_s)} \tag{2.30}$$

Using inverse Laplace transformation on (2.29) and (2.30), the primary and the snubber currents can be expressed as follows.

$$i_p(t) \approx nI_o - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{(C_a+C_s)}}} \tag{2.31}$$

$$i_a(t) \approx \frac{V_{dc}C_a}{\sqrt{L(C_a + C_s)}} + \frac{V_{dc}C_s}{\sqrt{L(C_a + C_s)}}\left\{1 - \cos\left(\frac{1}{\sqrt{L_aC_s}}(t - t_4)\right)\right\} - \Delta_{L_m}(t - t_4) \tag{2.32}$$

So, the voltage v_s' can be expressed as

$$\begin{aligned} v_s'(t) &= V_{dc} + \frac{1}{C_s}\int_{t_4}^{t}(i_p(t) - i_a(t) - i_s(t))dt \\ &\approx V_{dc}\left\{1 + \sqrt{\frac{L_aC_s}{L(C_s+C_a)}}\sin(\frac{1}{\sqrt{L_aC_s}}(t-t_4))\right\} \end{aligned} \tag{2.33}$$

If L is sufficiently large than L_a, the snubber circuit carries most of the current responsible for the ringing of v_s', back to the source. The snubber is in a regenerative state during this interval.

A closer observation of (2.33) shows that the peak voltage overshoots depend on the ratio of L_a and L. The parasitic capacitance of the secondary and snubber diode bridges also affect these oscillations. The peak voltage cannot go more than

$$\Delta V_s' = V_{dc}\sqrt{\frac{L_aC_s}{L(C_s+C_a)}}$$

Thus the voltage overshoots can be reduced significantly if $L_a \ll L$.
The high-frequency oscillations in the voltage v_s and snubber current i_a die down due to various losses in the power and snubber circuits. Thus, the state variables can further be approximated as follows.

$$v_s'(t) \approx V_{dc} \tag{2.34}$$

$$i_p(t) \approx nI_o - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{(C_a+C_s)}}} \tag{2.35}$$

$$i_a(t) \approx \frac{V_{dc}}{\sqrt{\frac{L}{(C_a+C_s)}}} - \Delta_{L_m}(t-t_4) \tag{2.36}$$

This mode ends with switching OFF the device Q_1, and the time interval can be calculated as

$$t_V = t_5 - t_4 = \frac{d}{2f_s} - t_I - t_{II} - t_{III} - t_{IV} \tag{2.37}$$

Where the applied duty ratio d is defined as the ratio of the time interval between the switching of the two legs to half the switching period $T_s/2$. The time taken for the snubber current to fall may be less than, equal to or more than t_V. However, to make the analysis simple, it is assumed that the time taken for i_a to fall to zero is t_V, i.e. in steady state, $2I_m \approx \frac{V_{dc}}{\sqrt{\frac{L}{C_a+C_s}}}$. Therefore, with the above assumptions, the state variables at the end of the active mode are as follows.

$$i_p(t_5) \approx nI_o - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{C_a+C_s}}}$$

$$i_a(t_5) \approx 0$$
$$v_s'(t_5) \approx V_{dc}$$

The magnetising current at the end of the mode is,

$$i_m(t_5) = I_m \approx -I_m + \frac{V_{dc}}{\sqrt{\frac{L}{C_a+C_s}}}$$

Section 2.5 presents a detailed discussion about this mode if the time taken for i_a to reach zero is less than t_V.

2.2.6 Mode 6 (Leading Leg Switching)

Fig 2.10 shows the fourth-order circuit formed after turning off the device Q_4. The initial conditions of state variables are $i_p(t_5) \approx nI_o - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{C_a+C_s}}}$, $i_a(t_5) \approx 0$, $v_s'(t_5) \approx V_{dc}$, and $v_a(t_5) = V_{dc}$. Current i_p starts charging and discharging of C_4 and C_3, respectively. The

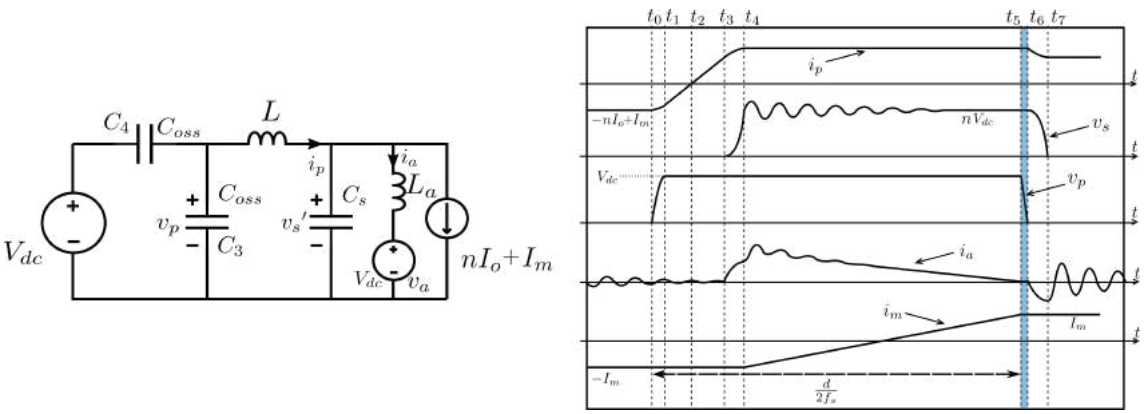


Fig. 2.10: Equivalent circuit for Mode 6.

current i_m is assumed to be constant at I_m. Solving the equivalent circuit using Laplace

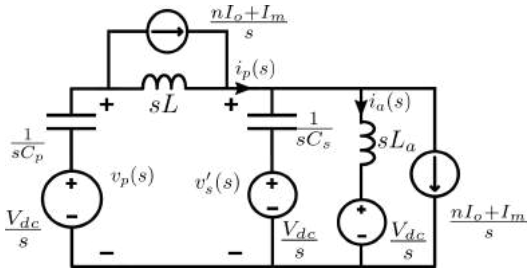


Fig. 2.11: Equivalent Laplace transformation circuit for Mode 6.

transformation as shown in Fig 2.11, we get

$$i_p(s) = \frac{\left(nI_o - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{C_s+C_a}}}\right)\left(L + \frac{Z_2(s)}{s}\right)}{sL + \frac{1}{sC_p} + Z_2(s)}$$

Where $Z_2(s) = \frac{sL_a}{1+s^2L_aC_s}$. Approximation of the above expression using $L \gg L_a$ and taking inverse Laplace transform of it gives

$$i_p(t) \approx \left(nI_o - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{C_a+C_s}}}\right)\cos\left(\frac{1}{\sqrt{LC_p}}(t-t_5)\right) \tag{2.38}$$

Using (2.38), the pole voltage v_p can be expressed as follows.

$$\begin{aligned} v_p(t) &= V_{dc} - \frac{1}{C_p}\int i_p(t)dt \\ &\approx V_{dc} - \left(nI_o - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{C_a+C_s}}}\right)\sqrt{\frac{L}{C_p}}\sin\left(\frac{1}{\sqrt{LC_p}}(t-t_5)\right) \end{aligned} \tag{2.39}$$

The snubber current is obtained as follows.

$$i_a(s) = \frac{i_p(s) - \frac{nI_o+I_m}{s}}{1+s^2L_aC_s} \tag{2.40}$$

Applying $L \gg L_a$ and finding inverse Laplace transformation, we get

$$i_a(t) \approx \left(nI_o - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{(C_a+C_s)}}}\right)\left\{\cos\left(\frac{1}{\sqrt{LC_p}}(t-t_5)\right) - 1\right\} \tag{2.41}$$

Then, the primary referred secondary voltage can be written as

$$v_s'(t) = \frac{1}{C_s}\int_{t_5}^{t}[i_p(t) - i_a(t) - nI_o - I_m] \tag{2.42}$$

Thus using (2.38) and (2.41) in (2.42),

$$v_s'(t) \approx V_{dc} \tag{2.43}$$

The mode ends with v_p getting clamped to zero and reverse biasing the diode D_4. Therefore the time taken for the completion of this transition is

$$t_{VI} = t_6 - t_5 = \sqrt{LC_p}\sin^{-1}\left(\frac{V_{dc}\sqrt{C_p}}{(nI_o - I_m)\sqrt{L} + V_{dc}\sqrt{C_a+C_s}}\right) \tag{2.44}$$

Though, practically $\sin\left(\frac{1}{\sqrt{LC_p}}(t_6 - t_5)\right) \approx \frac{t_{VI}}{\sqrt{LC_p}}$. Therefore v_p essentially decreases linearly as follows.

$$v_p(t) \approx V_{dc} - \left(nI_o - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{C_a+C_s}}}\right)\frac{1}{C_p}(t - t_5)$$

$$i_p(t) \approx nI_o - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{C_a+C_s}}}$$

$$i_a(t) \approx 0$$

So, time taken for the pole voltage to reach zero is

$$t_{VI} = t_6 - t_5 = \frac{V_{dc}C_p}{\left(nI_o - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{C_a+C_s}}}\right)}$$

Thus, at the end of this interval $v_p(t_6) = 0$, $i_p(t_6) \approx nI_o - I_m + \frac{V_{dc}}{\sqrt{L/(C_a+C_s)}}$, $v_s'(t_6) \approx V_{dc}$, and $i_a(t_6) \approx 0$.

2.2.7 Mode 7 (Secondary Voltage Fall)

Shorting the inverter bridge's pole terminals marks the beginning of C_a and C_s discharging. The fourth-order equivalent circuit shown in Fig 2.12 can be reduced to a second-order

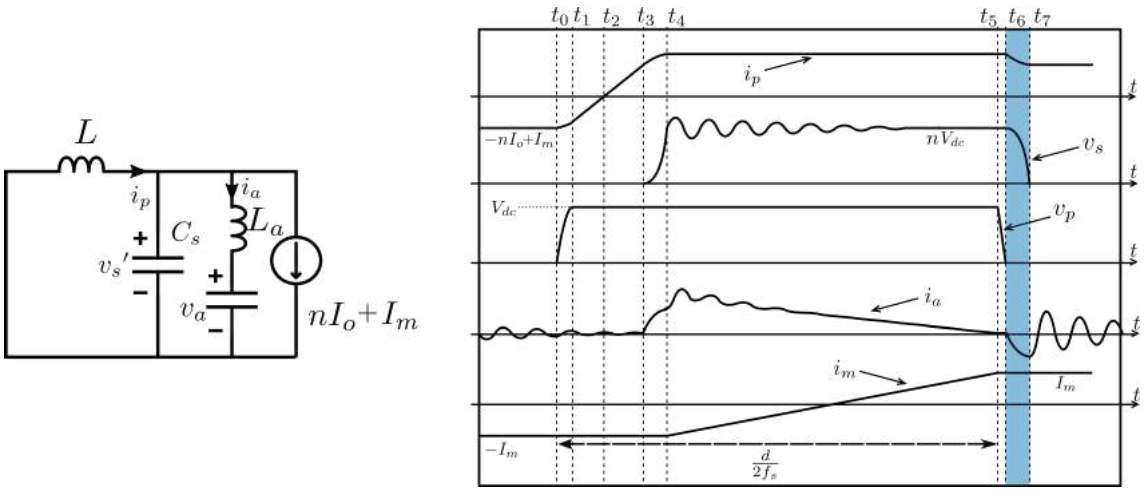


Fig. 2.12: Equivalent circuit for Mode 7.

circuit. The initial conditions of the circuit are $i_p(t_6) \approx nI_o - I_m + \frac{V_{dc}}{\sqrt{L/(C_a+C_s)}}$, $i_a(t_6) \approx 0$, $v_p(t) = 0$, and $v_s'(t_6) \approx V_{dc}$. And, the magnetising current i_m is assumed to be constant

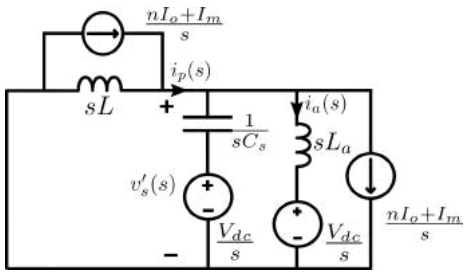


Fig. 2.13: Laplace transformation equivalent circuit for mode 7.

at I_m. Fig 2.13 shows the Laplace transformation equivalent circuit. Solving the circuit for current $i_p(s)$ gives

$$i_p(s) = \frac{nI_o + I_m}{s} - \frac{\frac{V_{dc}}{s}}{sL + Z(s)} \tag{2.45}$$

Where $Z(s) = \frac{1}{sC_s} || \left(\frac{1}{sC_a} + sL_a\right)$. Substituting $Z(s)$ in (2.45) and then taking the Laplace inverse shows

$$i_p(t) \approx nI_o - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{C_a+C_s}}} \left\{1 - \sin\left(\frac{1}{\sqrt{L(C_s+C_a)}}(t-t_6)\right)\right\} \tag{2.46}$$

To find $i_a(s)$

$$i_a(s) = \frac{\left(i_p(s) - \frac{nI_o+I_m}{s}\right)\frac{1}{sC_s}}{sL_a + \frac{1}{sC_a} + \frac{1}{sC_s}} \tag{2.47}$$

Taking Laplace inverse of (2.47), we get

$$i_a(t) \approx -\frac{V_{dc}C_a}{\sqrt{L(C_a+C_s)}} \sin\left(\frac{1}{\sqrt{L(C_s+C_a)}}(t-t_6)\right) \tag{2.48}$$

The converter voltages v_a and $v_s'(s)$ can be written as

$$v_a(t) = V_{dc} + \frac{1}{C_a}\int_{t_6}^{t} i_a(t)dt$$

$$v_s'(t) = V_{dc} + \frac{1}{C_s}\int_{t_6}^{t} \left[i_p(t) - i_a(t) - nI_o - I_m\right] dt$$

Solving the above two equations using (2.46) and (2.48),

$$v_s'(t) \approx v_a(t) \approx V_{dc} \cos\left(\frac{1}{\sqrt{L(C_s+C_a)}}(t-t_6)\right) \tag{2.49}$$

Voltage v_s' cannot go negative, as rectifier diodes would start conducting, shorting the secondary terminals of the transformer. Thus, the time required for the transition to end and v_s' to reach zero is

$$t_{VII} = t_7 - t_6 = \frac{\pi}{2}\sqrt{L(C_a+C_s)} \tag{2.50}$$

The state variables at the end of this mode are, $i_p(t_7) \approx nI_o - I_m$, $i_a(t_7) \approx -\frac{V_{dc}C_a}{\sqrt{L(C_a+C_s)}}$, and $v_a(t_7) \approx v_s'(t_7) = 0$.

2.2.8 Mode 8 (Zero State)

There is no power transfer from the source to the load during this mode. Fig 2.14 shows

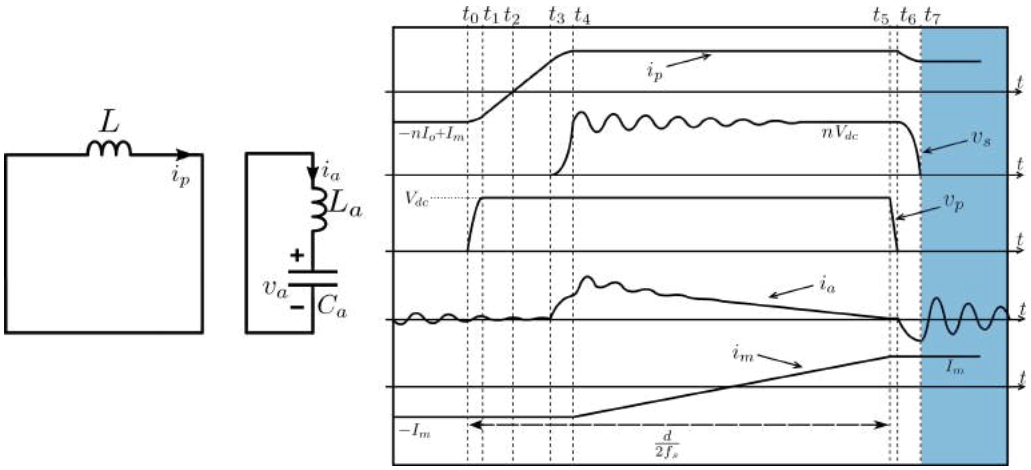


Fig. 2.14: Equivalent circuit for Mode 8

the equivalent circuit for the zero/passive state. Switches Q_1 and Q_3 are in conduction. The Kirchhoff's laws give the circuit state variables as follows.

$$L\frac{di_p(t)}{dt} = 0$$

$$C_a\frac{dv_a(t)}{dt} = i_a(t)$$

$$L_a\frac{di_a(t)}{dt} = -v_a(t)$$

Solving the above differential equations, we get

$$i_p(t) = nI_o - I_m \tag{2.51}$$

$$i_a(t) = -\frac{V_{dc}C_a}{\sqrt{L(C_a+C_s)}}\cos\left(\frac{1}{\sqrt{L_aC_a}}(t-t_7)\right) \tag{2.52}$$

Passive state ends with the turn-OFF of device Q_1. Time for this interval is given by

$$t_{VIII} = t_8 - t_7 = \frac{(1-d)}{2f_s} - t_{VI} - t_{VII} \tag{2.53}$$

The initial condition of snubber current leads to the above high-frequency oscillations in i_a. Owing to its small amplitude, high-frequency oscillations, and relatively long interval of passive and current commutation modes, we assume it would decay to zero in any of these intervals, i.e. before another switching instant.

2.3 Average Output Voltage

The average output voltage V_o is determined using the closed-form expressions for each mode's primary referred secondary voltage v_s'.

$$\frac{V_o}{n} \approx 2f_s \left[\int_0^{T_s/2} v_s'(t)dt\right]$$

$$\frac{V_o}{n} \approx 2f_s \left[\int_0^{t_{IV}} V_{dc}\left\{1-\cos\left(\frac{1}{\sqrt{L(C_s+C_a)}}t\right)\right\}dt + \int_0^{t_V} V_{dc}dt + \int_0^{t_{VI}} V_{dc}dt + \int_0^{t_{VII}} V_{dc}\cos\left(\frac{1}{\sqrt{L(C_s+C_a)}}t\right)dt\right]$$

Using (2.50) and (2.24), $t_{IV} = t_{VII}$. Therefore,

$$\frac{V_o}{n} \approx 2f_s V_{dc}\left[\frac{d}{2f_s} - t_I - t_{II} - t_{III} + t_{VI}\right] \tag{2.54}$$

equating (2.9), (2.12), (2.15), and (2.44) in (2.54), we get

$$V_o \approx ndV_{dc} - 2nf_sL(nI_o - I_m)\left[1+\sqrt{1-\left(\frac{V_{dc}\sqrt{C_p}}{(nI_o-I_m)\sqrt{L}}\right)^2}\right] - \frac{nV_{dc}}{\pi}\left(\frac{f_s}{f_1}\right)\left[\sin^{-1}\left(\frac{V_{dc}\sqrt{C_p}}{(nI_o-I_m)\sqrt{L}}\right) - \sin^{-1}\left(\frac{V_{dc}\sqrt{C_p}}{(nI_o-I_m)\sqrt{L}+V_{dc}\sqrt{C_a+C_s}}\right)\right]$$

Neglecting the magnetising current I_m w.r.t. primary referred load current nI_o, we can further simplify the above converter gain expression as follows.

$$V_o \approx ndV_{dc} - 2n^2f_sLI_o\left[1+\sqrt{1-\left(\frac{V_{dc}\sqrt{C_p}}{nI_o\sqrt{L}}\right)^2}\right] - \frac{nV_{dc}}{\pi}\left(\frac{f_s}{f_1}\right)\left[\sin^{-1}\left(\frac{V_{dc}\sqrt{C_p}}{nI_o\sqrt{L}}\right) - \sin^{-1}\left(\frac{V_{dc}\sqrt{C_p}}{nI_o\sqrt{L}+V_{dc}\sqrt{C_a+C_s}}\right)\right] \tag{2.55}$$

Where $2\pi f_1 = 1/\sqrt{LC_p}$. The first term in (2.55) gives the ideal output voltage. The second term corresponds to the duty loss introduced by the leakage inductance during the current commutation. The third term introduces the voltage loss and gain due to lag and lead leg switching. However, it always results in voltage loss of ≥ 0 because L stores higher magnetic energy during lead-leg switching than lag-leg. It leads to a faster transition when going from active to zero states. Thus, the voltage gain is lesser than the loss. The third term cannot be neglected if f_s and f_1 are comparable, especially at smaller load conditions. The leakage inductance of the snubber transformer does not affect the overall converter gain. The effect of snubber bridge parasitic capacitance would be reduced at higher loads such that $nI_o \gg \frac{V_{dc}}{\sqrt{L/(C_s+C_a)}}$.

2.4 Snubber Non-Idealities

An ideal snubber consists of a snubber transformer with zero leakage inductance ($L_a = 0$) and diode bridge with no parasitic capacitance ($C_a = 0$). It clamps the secondary voltage overshoots to nV_{dc} with minimum snubber losses. Section 2.2 discusses the operation of PSFB and the proposed snubber considering these two significant parasitics, L_a and C_a. (2.56) shows the maximum voltage overshoot in voltage v_s' as

$$\Delta V_s' = V_{dc}\sqrt{\frac{L_a C_s}{L(C_s + C_a)}} \tag{2.56}$$

The proposed snubber is a regenerative passive snubber. However, the regenerative action of the snubber is only during the active state. The current flowing in the zero state only leads to power loss in the snubber. The snubber current i_a in the zero state is expressed as

$$i_a(t) = \pm\frac{V_{dc}C_a}{\sqrt{L(C_a + C_s)}}\cos\left(\frac{1}{\sqrt{L_a C_a}}t\right) \tag{2.57}$$

2.4.1 Effects of Snubber Transformer Leakage Inductance L_a

The frequency of ringing in v_s' and in current i_a depend on the leakage inductance L_a. A smaller L_a leads to high-frequency ringing, which leads to faster decay in the oscillations due to increased resistance. Equation (2.56) shows that the secondary voltage overshoot is directly dependent on the squared root of the L_a/L ratio. It establishes that the smaller the percentage of L_a to L, the smaller the voltage overshoot. The magnitude of L depends on the ZVS requirement of the converter and doesn't have any independent control. However, L_a doesn't affect the converter operation except for the high-frequency ringing and the voltage overshoots. Therefore, L_a is desired to be as small as possible.

2.4.2 Effects of Snubber Bridge Capacitance C_a

Equation (2.56) shows that the snubber diode's junction capacitance C_a is responsible for the further reduction of the secondary voltage as a higher C_a would lead to a smaller $\delta_{v_s'}$. But, (2.57) shows that a larger C_a leads to a larger amplitude of the current i_a in the passive state, which would result in higher snubber losses. A snubber with minimum losses is preferred when reduction of L_a can reduce these voltage overshoots. Therefore, the snubber diodes with minimum junction capacitance are preferred.

2.5 Deviations from the Analysis

Section 2.2.5 discusses the converter operation in active mode, considering a finite magnetising inductance and no ripple in the output current I_o. It was also assumed that the snubber current i_a linearly falls to zero in time t_V to simplify the analysis. However, in a practical converter, the output current I_o has ripple ΔI_o. Also, the time taken for

i_a to fall may be less or more than what was considered in Section 2.2.5. This section presents a detailed analysis of snubber current falling to zero before t_5. Fig 2.15(a) shows

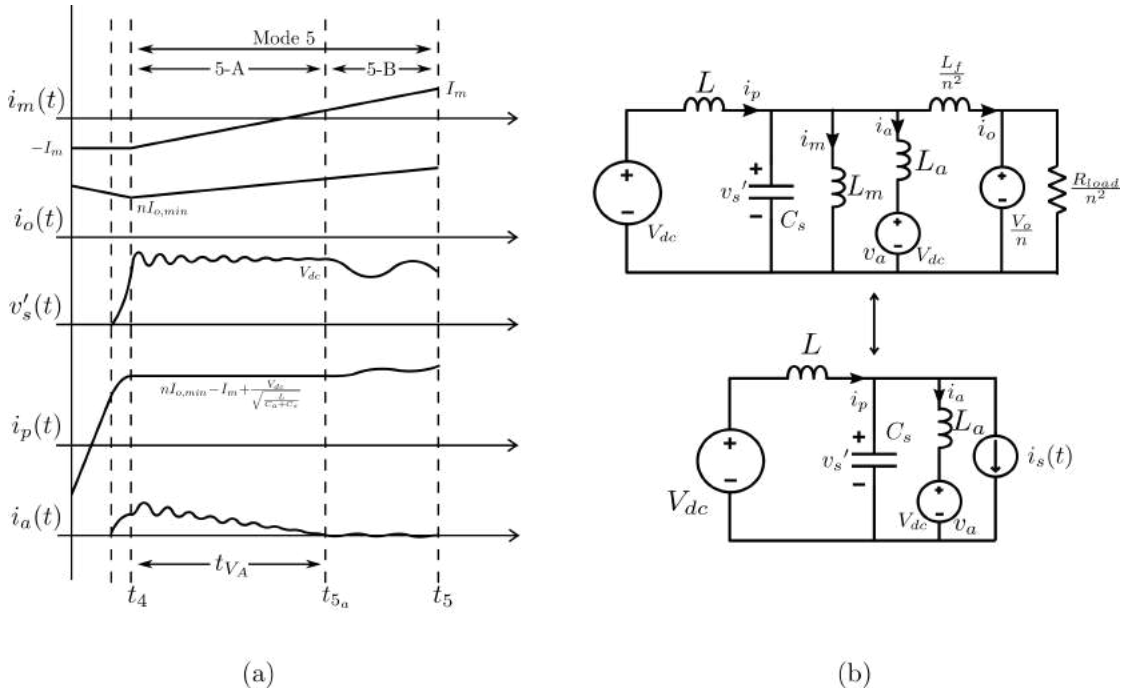


Fig. 2.15: (a) Converter state variables considering the output current ripple and finite magnetising inductance. (b) Transformation of the filter and magnetising inductance to a ramping current sink.

the different state variables during modes 3, 4, and 5. The filter inductance referred to primary and magnetising inductances of the transformers are large compared to L and L_a. Thus magnetising current and reflected output current during mode 4 are assumed to be reasonably constant at $-I_m$ and $nI_{o,min}$, respectively. Where $I_{o,min} = I_o - \frac{\Delta I_o}{2}$. Further, L_f and L_m can be replaced by ramping current sinks in the equivalent circuit for mode 5. Fig 2.15(b) shows the transformation of the two inductances to a current sink. The ramping current sink can be expressed as in (2.58).

$$i_s(t) = -I_m + nI_{o,min} + \Delta_s(t - t_4) \tag{2.58}$$

Where $\Delta_s = \Delta_{L_m} + \frac{n(nV_{dc} - V_o)}{L_f}$. L_f is the filter inductance, while $\Delta_{L_m} = V_{dc}/L_m$, and L_m is the parallel combination of the magnetising inductance of the two transformers.

2.5.1 Sub-mode 5-A (Snubber Current Fall)

Fig 2.16 shows the equivalent circuit for sub-mode 5-A. Initial conditions of the state variables are: $i_p(t_4) = -I_m + nI_{o,min} + \frac{V_{dc}}{\sqrt{L/(C_s+C_a)}}$, $i_a(t_4) = \frac{V_{dc}C_a}{\sqrt{L(Cs+Ca)}}$, and $v_s'(t_4) = V_{dc}$.

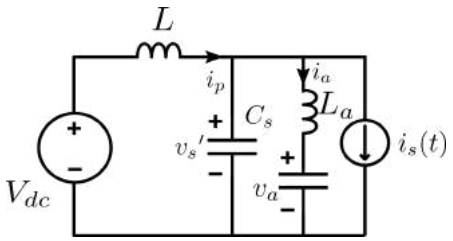


Fig. 2.16: Sub-mode 5-A equivalent circuit.

The circuit is solved in a similar manner as was solved in Section 2.2.5. The converter state variables obtained are as follows.

$$i_p(t) \approx -I_m + nI_{o,min} + \frac{V_{dc}}{\sqrt{\frac{L}{C_a+C_s}}} \tag{2.59}$$

$$i_a(t) \approx \frac{V_{dc}C_a}{\sqrt{L(C_a+C_s)}} + \frac{V_{dc}C_s}{\sqrt{L(C_a+C_s)}}\left\{1-\cos(\frac{1}{\sqrt{L_aC_s}}(t-t_4))\right\} - \Delta_s(t-t_4) \tag{2.60}$$

$$\begin{aligned} v_s'(t) &= V_{dc} + \frac{1}{C_s}\int (i_p(t) - i_a(t) - i_s(t))dt \\ &\approx V_{dc}\left\{1+\sqrt{\frac{L_aC_s}{L(C_s+C_a)}}\sin(\frac{1}{\sqrt{L_aC_s}}(t-t_4))\right\} \end{aligned} \tag{2.61}$$

Due to different losses during the active state, oscillations in the above-expressed currents and voltages die down to give simplified expressions (2.62).

$$\begin{aligned} v_s'(t) &\approx V_{dc} \\ i_p(t) &\approx -I_m + nI_{o,min} + \frac{V_{dc}}{\sqrt{\frac{L}{C_a+C_s}}} \\ i_a(t) &\approx \frac{V_{dc}}{\sqrt{\frac{L}{C_a+C_s}}} - \Delta_s(t-t_4) \end{aligned} \tag{2.62}$$

Time taken for the snubber current i_a to reduce to zero is stated as

$$t_{V_A} = \frac{V_{dc}}{\Delta_s}\sqrt{\frac{C_s+C_a}{L}} \tag{2.63}$$

2.5.2 Sub-mode 5-B

An another sub-mode 5-B is added if the current i_a falls to zero in time less than t_V. As i_a crosses zero to go negative, it discharges the capacitance C_a, forming a fourth-order

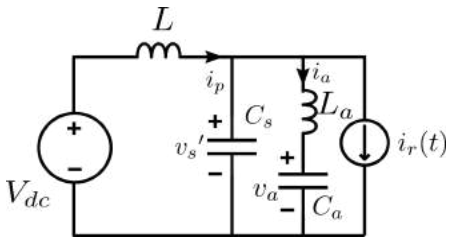


Fig. 2.17: Sub-mode 5-B equivalent circuit

resonant circuit as shown in Fig 2.17. The initial conditions of the state variables are $i_p(t_{5_a}) = nI_{o,min} - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{C_a+C_s}}}$, $v_s'(t_{5_a}) = V_{dc}$, $i_a(t_{5_a}) = 0$, and $v_a(t_{5_a}) = V_{dc}$. The ramping current sink $i_r(t)$ is expressed as (2.64).

$$i_r(t) = nI_{o,min} - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{C_a+C_s}}} + \Delta_s(t - t_{5_a}) \tag{2.64}$$

Let $I = nI_{o,min} - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{C_a+C_s}}}$. The converter variables are solved using KVL and KCL on the Laplace transformed equivalent circuit as shown in Fig 2.18.

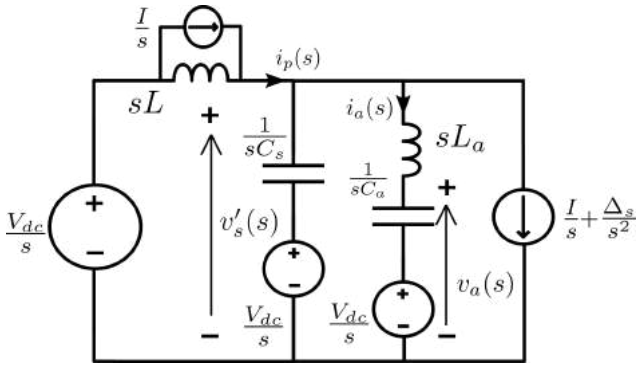


Fig. 2.18: Laplace transform equivalent circuit

$$i_p(s) = \frac{I}{s} + \frac{Z(s)\Delta_s}{s^2(Z(s) + sL)}$$

Equating $Z(s) = \frac{1}{sC_s} || \left(sL_a + \frac{1}{sC_a}\right)$ in the above expression, we get

$$\begin{aligned} i_p(s) &= \frac{I}{s} + \frac{\Delta_s(s^2L_aC_a + 1)}{s^2(1 + s^2L(C_a + C_s) + s^4LL_aC_sC_a)} \\ &\approx \frac{I}{s} + \frac{\Delta_s(s^2L_aC_a + 1)}{s^2(1 + s^2L(C_a + C_s) + s^4LL_aC_sC_a)} \end{aligned}$$

In view of the fact that $L_a \frac{C_s C_a}{(C_a+C_s)} \ll L(C_a + C_s)$,

$$i_p(s) \approx \frac{I}{s} + \frac{\Delta_s(s^2 L_a C_a + 1)}{s^2(1 + s^2 L(C_a + C_s))} \tag{2.65}$$

Snubber current $i_a(s)$ can be expressed as

$$i_a(s) \approx (i_p(s) - i_r(s)) \left(\frac{C_a}{s^2 L_a C_s C_a + (C_s + C_a)} \right) \tag{2.66}$$

Using (2.65) in (2.66), we get

$$i_a(s) \approx -\Delta_s \frac{C_a}{(C_s + C_a)\left(s^2 + \frac{1}{L(C_s+C_a)}\right)} \tag{2.67}$$

Inverse Laplace transformation of (2.65) and (2.67) give

$$i_p(t) \approx nI_{o,min} - I_m + \frac{V_{dc}}{\sqrt{\frac{L}{C_s+C_a}}} + \Delta_s \left\{ (t - t_{5a}) - \sqrt{L(C_a + C_s)} \sin\left(\frac{1}{\sqrt{L(Ca + C_s)}}(t - t_{5a})\right) \right\} \tag{2.68}$$

$$\begin{aligned} i_a(t) &\approx -\Delta_s C_a \sqrt{\frac{L}{C_a + C_s}} \sin\left(\frac{1}{\sqrt{L(Ca + C_s)}}(t - t_{5a})\right) \\ &\approx 0 \end{aligned} \tag{2.69}$$

$$\begin{aligned} v_s'(t) &= V_{dc} + \frac{1}{C_s} \int (i_p(t) - i_a(t) - i_s(t)) dt \\ &\approx V_{dc} + \Delta_s L \left\{ \cos\left(\frac{1}{\sqrt{L(C_a + C_s)}}(t - t_{5a})\right) - 1 \right\} \end{aligned} \tag{2.70}$$

2.5.3 Effects on the Converter Operation

The faster decay of the snubber current i_a reduces the RMS current flowing through the snubber circuit, reducing the conduction losses seen by the snubber. However, it comes with a disadvantage of average output voltage loss, as seen in the Sub-mode 5-B. A possible solution to overcome this disadvantage during the design process could be incorporating an approximate duty loss in the duty expression used in the design flow shown in Chapter 3.

2.6 Summary

The chapter presents a comprehensive analysis of the PSFB converter operation with the proposed snubber. Closed-form expressions for the state variables like main transformer's

primary current i_p, pole voltage v_p, secondary voltage v_s, and snubber current i_a are obtained for each operating mode.

The converter gain expression was obtained using these closed-form expressions, which would be helpful in designing the converter in the next chapter. Secondary bridge voltage overshoot is dependent on the squared root of L_a/L. A higher value of snubber bridge capacitance leads to a further reduction in the secondary voltage overshoot. However, it increases the RMS value of the i_a leading to higher snubber conduction losses.

The analysis assumes that the current i_a falls nearly around when the conducting switch of the leading leg is switched OFF to simplify the analysis. However, the chapter also analyses the deviation from the assumption. The last section of the Chapter discusses the deviation from this assumption and the reduction of converter gain if this fall time is less than the active mode interval.

Chapter3

Phase-Shifted Full-Bridge Design

3.1 Introduction

The previous chapter presents a detailed analysis of different modes of operation of the PSFB along with the proposed snubber. The study divides the operation into eight topological stages, considering the diode bridge capacitances and transformer leakage inductances. The converter gain was determined using the closed-form expressions obtained during each mode of operation. The chapter also establishes the minimum leakage inductance required and the limits on the dead time selection to achieve ZVS turn-ON.

This chapter presents a detailed design procedure for a PSFB converter with the proposed snubber. The design process is carried out for a step-down and a high output current PSFB. The goal of the design would be to achieve ZVS turn-ON in the entire range of load variation and assuming ten per cent change in the input voltage.

The chapter is arranged in the following order. Section 3.2 discusses the converter specifications and briefs about the objectives of the design process and the essential considerations related to it. In Section 3.3, the devices for the three bridges are selected, considering the ideal converter operation. The output capacitances are then obtained from the device datasheets. Section 3.4 exploits the converter gain expression to determine the leakage inductance L and transformer turns ratio n using the converter specifications and extracted parasitic capacitances. Once L and n are known, the dead time is selected in Section 3.5 to accomplish the goal of ZVS turn-ON for all operating points of the converter. Finally, the last section covers the output filter design.

3.2 PSFB Design with the Proposed Snubber

The purpose of the design would be to build a 400/48 V, 1.5 kW PSFB converter considering the proposed snubber. The DC-DC converter will achieve the desired output voltage of 48 V and accomplish ZVS turn-ON for a 10% change in input voltage in the output power range of 0.5-1.5 kW. Table 3.1 shows the desired specification for the PSFB. Due to

Table 3.1: Converter Specifications

Input Voltage (V_{dc})	Output Voltage (V_o)	Switching Frequency (f_s)	Output Power (P_o)
360-440 V	48 V	100 kHz	1.5 kW

variation in the output power and input voltage, the converter has four extreme operating

conditions.
1. Minimum input voltage ($V_{dc,min}$) and Minimum output power ($P_{o,min}$)
2. Minimum input voltage ($V_{dc,min}$) and Maximum output power ($P_{o,max}$)
3. Maximum input voltage ($V_{dc,max}$) and Maximum output power ($P_{o,max}$)
4. Maximum input voltage ($V_{dc,max}$) and Minimum output power ($P_{o,min}$)

However, two of the four extreme operating conditions mentioned above are redundant for the specific design objective of choosing n and L such that **(A)** and **(B)** discussed below are fulfilled. These design objectives should be satisfied in the entire load variation range, assuming ten per cent of input voltage variation.

(A) Achieve ZVS turn-On of all the inverter switches

Equation (3.1) gives us the criteria for minimum n^2L to achieve soft switching. It shows that the n and L determined for $V_{dc,max}$ and $P_{o,min}$ would also satisfy the requirement for other operating conditions.

$$n^2 L \geq C_p \left(\frac{V_{dc}}{I_o}\right)^2 \tag{3.1}$$

Where $I_o = P_o/V_o$.

(B) Achieve desired output voltage V_o

The required duty d to achieve specified V_o is determined as expressed as (3.2) using the converter gain expression in Section 2.3. Due to the boundary limits on the applied duty ratio, it is necessary to know the operating conditions which would lead to the minimum and maximum duty ratios. Practically, d is mainly dependent on the first two terms of 3.2 compared to the third term, which shows that for a given n and L, the duty required for $V_{dc,min}$ and $P_{o,max}$ would be greater than any other operating condition. While $V_{dc,max}$ and $P_{o,min}$ would lead to a duty smaller than any of the conditions.

$$\begin{aligned} d = \frac{V_o}{nV_{dc}} + \frac{2nf_sLI_o}{V_{dc}} \left[1 + \sqrt{1 - \left(\frac{V_{dc}\sqrt{C_p}}{nI_o\sqrt{L}}\right)^2}\right] \\ + 2f_s\sqrt{LC_p}\left[\sin^{-1}\left(\frac{V_{dc}\sqrt{C_p}}{nI_o\sqrt{L}}\right) - \sin^{-1}\left(\frac{V_{dc}\sqrt{C_p}}{nI_o\sqrt{L} + V_{dc}\sqrt{(C_a + C_s)}}\right)\right] \end{aligned} \tag{3.2}$$

Thus, if the two objectives satisfy the following cases, they would also fulfil all the other operating sets.

- $V_{dc,max}$ and $P_{o,min}$
- $V_{dc,min}$ and $P_{o,max}$

Design Flow Overview:

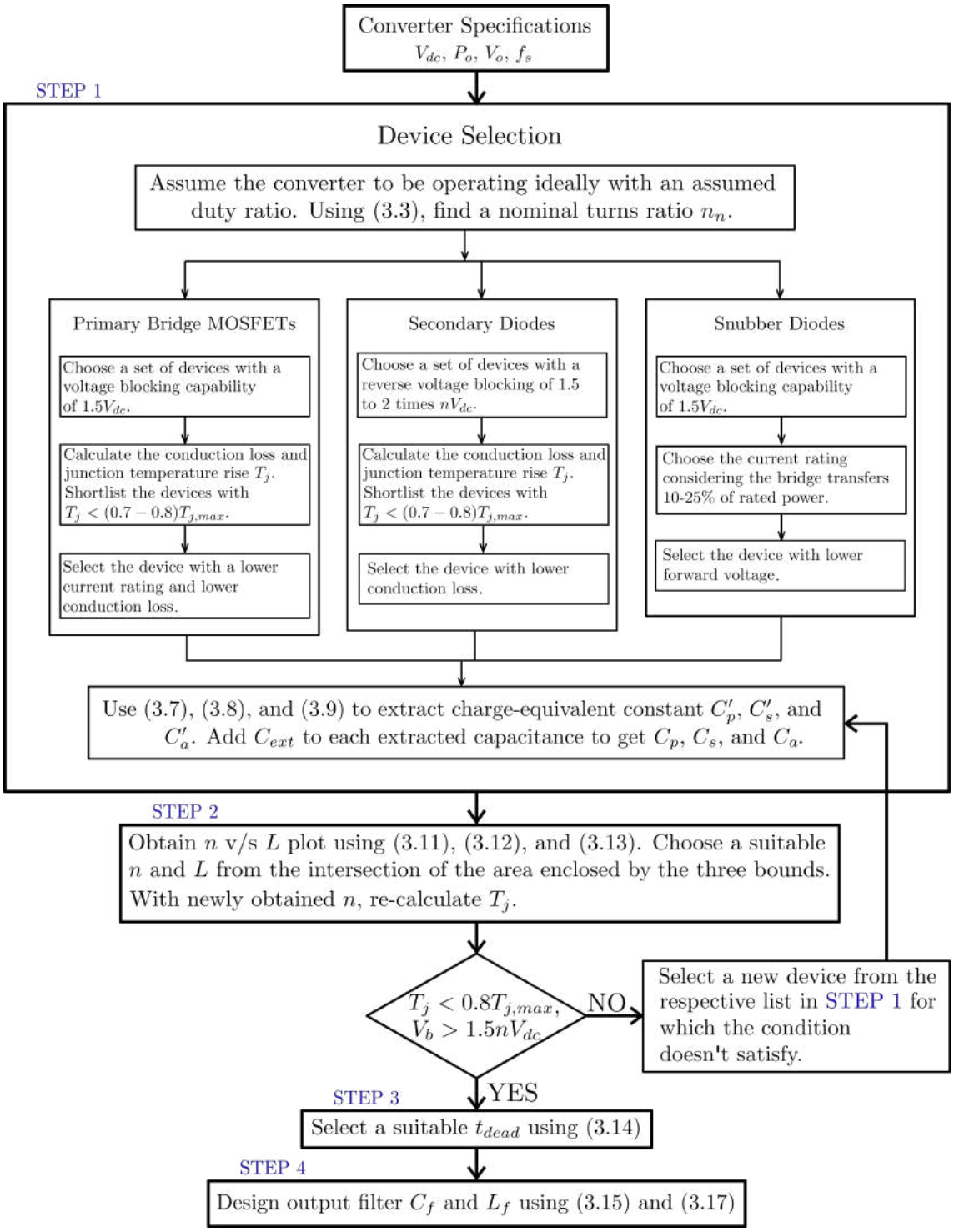


Fig. 3.1: PSFB Design Flow

Step 1: Based on conduction loss calculations, the primary, secondary, and snubber bridge devices are selected. We then extract output capacitances from their respective datasheets.

Step 2: Once we know the converter specifications and the device's capacitances, the aim is to determine L and n using (3.1) and (3.2) such that the design objectives are fulfilled.

Step 3: Selection of a dead time that results in soft turn-ON at all operating conditions.

Step 4: A low-pass filter for the PSFB converter is designed.

The following sections cover these design steps in detail. Fig 3.1 shows the flowchart for the design process.

3.3 Step 1: Selection of Devices and Extraction of Capacitances

To start with the design process, PSFB is assumed to be in ideal operation without the snubber. No parasitic capacitances and duty loss due to the leakage inductance are considered. Fig 3.2 shows the converter circuit and the associated waveforms when operating ideally. Primary device conduction loss calculation requires transformer turns ratio. Thus,

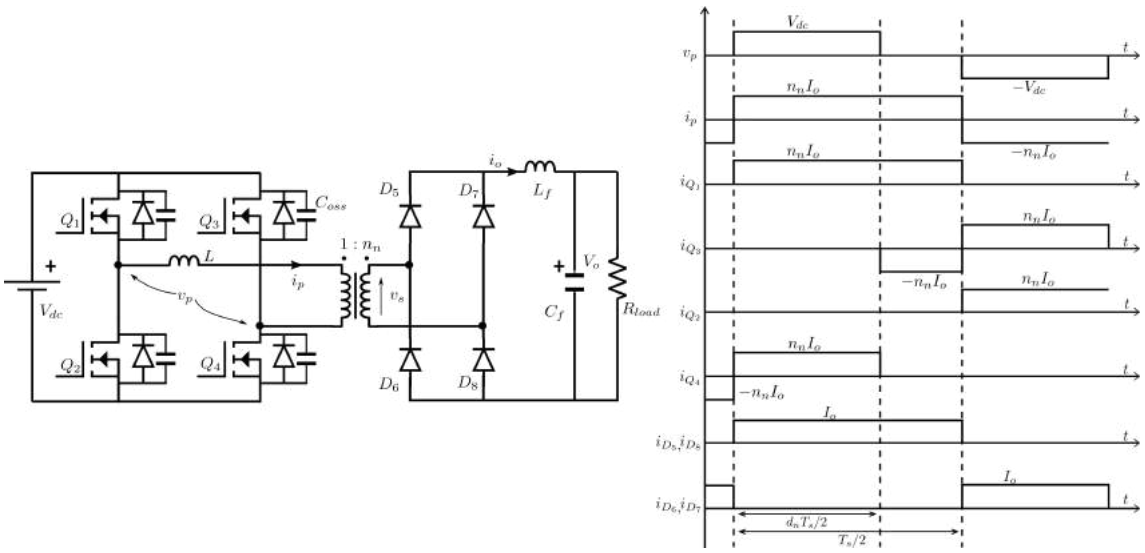


Fig. 3.2: Circuit diagram and associated waveforms of a PSFB converter without a snubber. It is assumed that the output current is constant at I_o. The duty loss due to leakage inductance L is neglected.

with the given specifications of DC input V_{dc} and output voltage V_o and an assumed nominal duty d_n, a nominal secondary to primary transformer turns ratio n_n is calculated as per the following:

$$n_n = \frac{V_o}{d_n V_{dc}} \tag{3.3}$$

For $d_n = 0.65$, $V_o = 48.48$ V, and $V_{dc} = 360$ V, the transformer turns ratio $n_n = 0.21$. Once we have calculated n_n, the rated output and input current can be calculated as follows:

$$I_o = P_o/V_o$$

Where, P_o is the rated output power and V_o is the output voltage. Thus, the rated load current referred to primary is $n_n I_o$. Considering the rated power of 1.5 kW, $I_o = 31.25$ A and $n_n I_o = 7.82$ A. Fig 3.2 shows the current flowing through the different devices.

3.3.1 Inverter Bridge Devices

Considering ZVS turn ON would ensure negligible switching losses, the preliminary selection of the primary devices is based on the conduction losses, junction temperature rise and output capacitance of the MOSFETs. 650 V, TO-247 package, silicon carbide devices are chosen.

Table 3.2: The ON-state resistance and output capacitance comparison of the devices.

Part No.	I_f (Rated)	R_{ds}@100°C	C_{oss}	P_Q (W)	R_{jc} (°C/W)	T_j (°C)
C3M0120065D	22 A	132 mΩ	45 pF	4.0392	1.53	98.2
C3M0120065K	22 A	132 mΩ	45 pF	4.0392	1.53	98.2
C3M0060065K	37 A	66 mΩ	80 pF	2.0196	0.99	93
C3M0045065K	49 A	49.5 mΩ	101 pF	1.5147	0.66	92.1

Conduction losses and junction temperature rise: Conduction loss P_Q per switch can be calculated using (3.4) as follows.

$$P_Q = I_{Q,rms} \times R_{ds} \tag{3.4}$$

Where $I_{Q,rms}$ is the RMS current through the switches and is expressed as

$$\begin{aligned} I_{Q,rms} &= \frac{n_n I_o}{\sqrt{2}} \\ &= 5.53\,\text{A} \end{aligned}$$

Considering the heat sink temperature at 90° C, the junction temperature rise T_j was found.

$$T_j = 90 + (R_{jc} + R_{cs}) \times P_Q \tag{3.5}$$

Where, R_{jc} and $R_{cs} = 0.5$°C/W are the junction-case and case-sink thermal resistances. A list of devices from wolfspeed are shown in Table 3.2 with their junction temperature

rise T_j less than 75% of the rated maximum value of $T_{j,max} = 175°C$.

Among the devices in Table 3.2, CREE's C3M120065K is chosen for the primary bridge owing to the following reasons.

- The devices with the Kelvin source pin have negligible common source inductance and therefore decouple the gate and the power circuits, which results in lower switching loss. Thus the four-terminal MOSFETs give better switching performance than the three-pin MOSFETs.
- As shown in Table 3, higher current rated devices have lower ON-state resistance R_{ds}, leading to lower conduction losses. However, the output capacitance C_{oss} of the MOSFETs increases with the increase in the current rating. Thus, the total equivalent capacitance C_p seen from the pole-point is larger for the higher current rated devices. This reduces range of soft switching or leads to the selection of a larger value of series inductance L as shown in Section 2.2.1. The selection of larger L results in higher duty loss at higher load currents.
  Also, it has been shown that around 10% of stored energy in output capacitances gets dissipated during the charging and discharging process [25]. Thus, devices with higher C_{oss} incur a higher losses than the devices with lower output capacitance.

Consequently, the devices with lower current ratings are chosen for the inverter bridge.

3.3.2 Secondary Bridge Diodes

Si Schottky diodes are used as the switching performance is better than Si diodes due to no reverse recovery effect. Theoretically, Schottky diodes have zero switching losses. Table 3.3 contains the TO-247 package diodes with a reverse voltage blocking capability of 200 V i.e more than $2n_n440$ V. Only two of the four diodes conduct simultaneously and

Table 3.3: Power dissipation table of different 200 V Si Schottky diodes.

Part No.	I_d (Rated)	R_d@125° C	V_f (V)	P_D (W)	R_{jc} (° C/W)	T_j (°C)
DSA90C200HR	90 A	10 mΩ	0.7	13.03	0.7	105.6
APT30S20BCTG	90 A	5 mΩ	0.7	11.8	0.58	102.8
DSA70C200HB	70 A	10 mΩ	0.75	13.8	0.7	106.5
DSSK 60-02AR	60 A	6.25 mΩ	0.7	12.1	0.66	105.8

will be conducting for half the switching cycle as shown in Fig 3.2. The average and RMS current values through each diode are given as follows:

$$I_{d,avg} = \frac{I_o}{2}$$
$$I_{d,rms} = \frac{I_o}{\sqrt{2}}$$

For $I_o = 31.25$ A, $I_{d,avg} = 15.625$ A and $I_{d,rms} = 22.1$ A. Power loss through each diode can be calculated as

$$P_D = V_f \times I_{d,avg} + R_d \times I_{d,rms}^2 \tag{3.6}$$

Where V_f and R_d are forward voltage and ON-state resistance of the diodes. The junction temperature rise T_j can be calculated as in (3.5). Due to its lower conduction losses and availability, IXYS's DSSK 60-02AR is used to build the rectifier bridge. The 3-pin TO-247 package consists of two common cathode diodes, each having a current rating of 30 A. These two diodes are used in parallel connections.

3.3.3 Snubber Bridge Diodes

The snubber bridge is designed considering that the snubber circuit transfers 10-25% of the rated output power. To reduce the switching losses schottky barrier diodes with a voltage blocking capability of 650 V are chosen to build the snubber diode bridge. Wolfspeed's E3D20065D was selected due to the unavailability of lower current rating devices, which is a 20 A rated device with a forward voltage of $V_f = 1$ V and ON-state resistance of $R_d = 50$ mΩ at 25°C and 1 A of current through the device. The 3-pin TO- 247 package consists of two common cathode diodes, each having a current rating of 10 A. These two diodes are used in parallel connections.

3.3.4 Extraction of Capacitances

This section presents the extraction of the output capacitances C_p', C_s', and C_a' through the device datasheets using charge equivalence methodology. It is noteworthy that C_p', C_a', and C_a' are the datasheet extracted device capacitances and not equal to the capacitances C_p, C_a, and C_s discussed in Chapter 2. The relationship between the two is discussed at the end of this section.

A. MOSFETs Output Capacitance:
The output capacitance of the MOSFET is dependent on the voltage across the devices, as shown in Fig 3.3. However, during the switching of the leg, the voltage increases across one and decreases across the other switch. Fig 3.3 shows the two output capacitances during an inverter leg switching. Assume that C_1 and C_2 are charged to V_{dc} and zero, respectively, just before the switching. The total capacitance C_p' seen by the pole terminals is the sum of the two capacitances. Fig 3.3 shows the capacitance variation of the high and low side MOSFETs with regard to v_p. The yellow curve shows the capacitance variation of C_p'. This capacitance is fairly constant for most of the variation in v_p. Also, [26] shows that energy due to stored charge in the MOSFETs needs to be considered to determine the energy required for soft-switching. The charge equivalent capacitance C_{Qeq} calculated for C3M120065K is expressed in (3.7).

$$C_{Qeq} = \frac{\int_0^{V_{dc}} [C_{oss}(v_p) + C_{oss}(V_{dc} - v_p)] dv_p}{V_{dc}} = 160.7\,\text{pF} \tag{3.7}$$

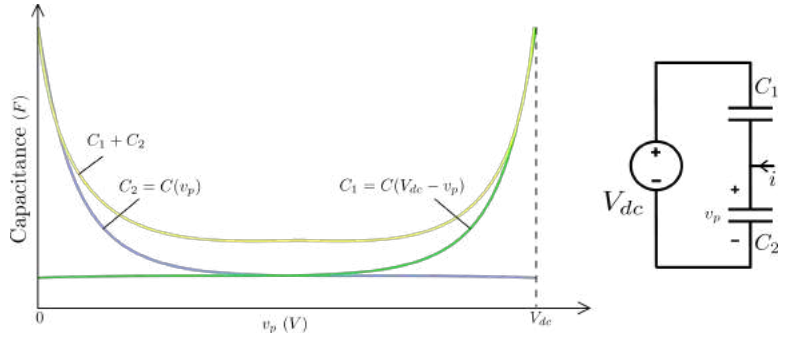


Fig. 3.3: The charging-discharging behaviour of the high and low side MOSFETs.

Where $C_{oss}(v_p)$ is the voltage-dependent capacitance obtained from the MOSFET datasheet. The constant capacitance C'_p is approximately equal to C_{Qeq}.

B. Secondary Bridge Diodes Junction Capacitance:
Let us assume that the current $i_s < I_o$ and all the diodes of the diode bridge are in conduction. The initial voltage of C_6 and C_7 is zero such that $v_s = 0$. As i_s reaches I_o, the equivalent circuit of the diode bridge is shown in Fig 3.4. A further increase in

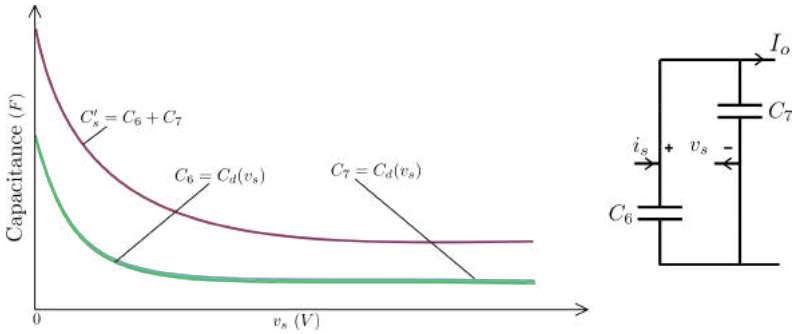


Fig. 3.4: Junction Capacitance vs reverse voltage characteristics of the secondary diode bridge.

i_s charges the diode capacitance C_6 and C_7. These junction capacitances are non-linear with regard to the reverse voltage seen by the diodes as shown in Fig 3.4. The total capacitance C'_s seen by the AC link of the diode bridge is the sum of C_6 and C_7, which is voltage-dependent as well. However, to fit our analysis and simplify the extraction of capacitance, we have considered the total capacitance C'_s equal to the charge equivalent capacitance $C_{d,Qeq}$, calculated as follows.

$$C_{d,Qeq} = \frac{\int_0^{V_b} 2C_d(v_s)dv_s}{V_b} = 1371.22\,\text{pF} \tag{3.8}$$

Where $C_d(v_s)$ is the voltage-dependent capacitance obtained from the DSSK 60-02A datasheet.

C. Snubber Bridge Diodes Junction Capacitance:
Before the rise of secondary voltage v_s and consequently v_a, current i_a is zero. Thus, all the snubber-diode junction capacitances C_{a1}, C_{a2}, C_{a3}, and C_{a4} are initially charged at $V_{dc}/2$ such that $v_a = 0$. As v_a increases, there is a simultaneous charging of C_{a2} and C_{a3} and discharging of C_{a1} and C_{a4}. This charging and discharging of the capacitances end with v_a getting clamped to V_{dc}. Fig 3.5 shows the equivalent circuit of the snubber

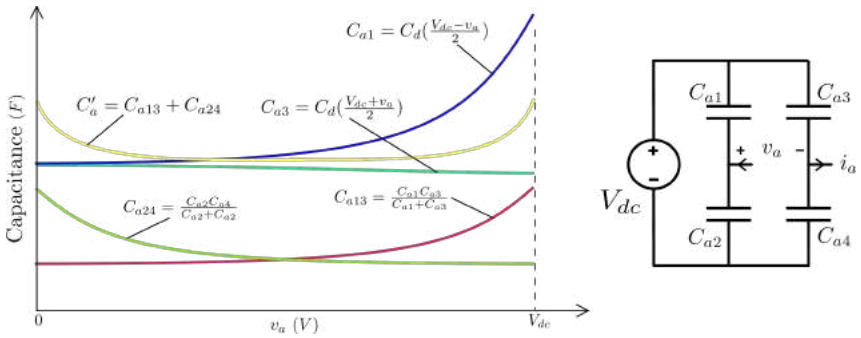


Fig. 3.5: Simultaneous charging and discharging of snubber bridge capacitances.

bridge during the transition. C_{a1} and C_{a2} are in series with C_{a3} and C_{a4}, respectively. Fig 3.5 shows the capacitance vs reverse voltage characteristics of C_{a1} and C_{a3}. C_{a13} is the series combination of the two capacitances. Similarly, C_{a24} is the series combination of C_{a2} and C_{a4}. Since there is a simultaneous charging and discharging of the capacitances, the total parasitic capacitance seen by the AC link of the snubber bridge is nearly constant and given by $C'_a = C_{a13} + C_{a24}$. The charge equivalent capacitance expressed in (3.9) is approximately equal to C'_a.

$$C_{a,Qeq} = \frac{\int_0^{V_{dc}} C'_a(v_a)dv_a}{V_{dc}} = 70.25\,\text{pF} \tag{3.9}$$

Where $C'_a(v_a)$ is calculated as discussed above and the capacitances vs reverse voltage curves of junction capacitances C_{a1}, C_{a1}, C_{a1}, and C_{a1} are obtained from the E3D20065D datasheet.

The constant capacitances extracted from the device datasheets are $C'_p = 160.7$ pF, $C'_s = 1371.22$ pF, and $C'_a = 70.25$ pF. It is noteworthy that parasitic capacitances due to PCB layout and heat sinks add to these datasheet extracted capacitances. The final capacitances that are required in the next section are given by

$$\begin{aligned} C_p &= C'_p + C_{ext} \\ C_s &= n^2(C'_s + C_{ext}) \\ C_a &= C'_a + C_{ext} \end{aligned} \tag{3.10}$$

Practically the external capacitance C_{ext} added to each of the three extracted capacitances would be different depending on the layout but is considered the same for all the three to simplify the design.

3.4 Step 2: Determine Transformer Turns Ratio n and Leakage Inductance L

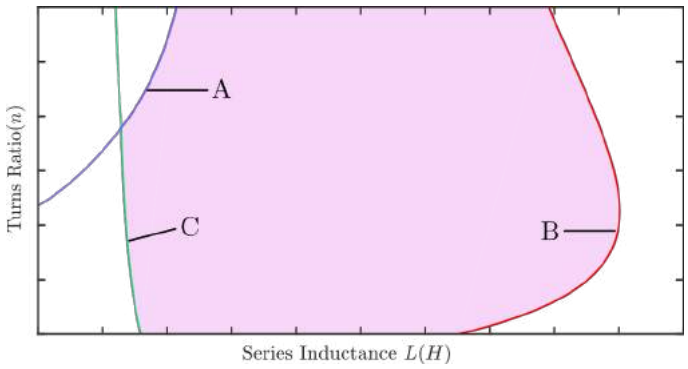


Fig. 3.6: n v/s L plot with the three constraints for a given V_{dc} and I_o, i.e. at a single operating point.

In the previous section, we extracted the values of parasitic capacitances from the device datasheets. This section will determine the transformer turns ratio n and leakage inductance L using the following two equations.

$$n^2 L \geq C_p \left(\frac{V_{dc}}{I_o}\right)^2 \tag{3.11}$$

Where C_p is the primary capacitance obtained in the previous section, V_{dc} is the input DC bus voltage, and I_o is the average output current. This constraint on the determination of n and L is due to the ZVS turn-ON requirement obtained in Section 2.2.1.

The duty d required to achieve a specified output voltage V_o can be expressed as a function of converter specifications V_{dc}, V_o, I_o, f_s and other parameters C_p, C_s, C_s, L and, n using the converter gain expression in Section 2.3.

$$\begin{aligned} d = \frac{V_o}{nV_{dc}} + \frac{2nf_s L I_o}{V_{dc}} \left[1 + \sqrt{1 - \left(\frac{V_{dc}\sqrt{C_p}}{nI_o\sqrt{L}}\right)^2}\right] \\ + 2f_s\sqrt{LC_p}\left[\sin^{-1}\left(\frac{V_{dc}\sqrt{C_p}}{nI_o\sqrt{L}}\right) - \sin^{-1}\left(\frac{V_{dc}\sqrt{C_p}}{nI_o\sqrt{L} + V_{dc}\sqrt{(C_a + C_s)}}\right)\right] \end{aligned} \tag{3.12}$$

However, the duty must not exceed the practical limits on the duty ratio. Thus,

$$d_{max} \geq d \geq d_{min} \tag{3.13}$$

Using (3.11), (3.12), and (3.13), we get the three constraints on the selection of n and L. The intersection of the three bounds gives us an infinite set of n and L. Fig 3.6 shows this region of interest coloured in pink. The area is bounded by the three curves, A, B and C. The curves A and B are obtained by equating $d = d_{min}$ and $d = d_{max}$, respectively. While the curve C is obtained using (3.11).

L and n for $V_{dc} \in [V_{dc,min}, V_{dc,max}]$ and $P_o \in [P_{o,min}, P_{o,max}]$:
In the above discussion, n and L can be determined considering the converter is designed for a single operating point. However, the design objective of the PSFB is to get a soft turn-ON and specified converter gain considering an input voltage regulation of 10% in the output power range of $0.5 - 1.5$ kW. As argued in Section 3.2, the design objectives are fulfilled for all operating points if they are satisfied for the two extreme conditions. The region of interest now becomes the intersection of the two areas obtained for the mentioned extreme conditions.
Table 3.4 comprises the parameters used to obtain the four plots in Fig 3.7 for the two extreme operating conditions. Table 3.5 shows the different external parasitic capacitances C_{ext} added to the extracted capacitances C_p', C_s', and C_a' using device datasheets.

Table 3.4: Paramters used to obtain the four plots using two extreme operating conditions.

	Condition I $V_{dc,min}$ and $P_{o,max}$	Condition II $V_{dc,max}$ and $P_{o,min}$
V_{dc}	360 V	440 V
I_o	31.25 A	10 A
f_s	100 kHz	100 kHz
d_{min}	0.2	0.2
d_{max}	0.85	0.85
C_p (pF)	$160.7 + C_{ext}$	$160.7 + C_{ext}$
C_s (pF)	$n^2(1371.22 + C_{ext})$	$n^2(1371.22 + C_{ext})$
C_a (pF)	$70.25 + C_{ext}$	$70.25 + C_{ext}$

Table 3.5: External Parasitic capacitance added to datasheet extracted capacitances, for the four plots.

	Fig 3.7(a)	Fig 3.7(b)	Fig 3.7(c)	Fig 3.7(d)
C_{ext} (pF)	0	100	200	300

Fig 3.7 shows the n v/s L plots for the two extreme operating conditions with the shaded area as the region of interest. The four plots are for the different values parasitic capacitances C_p, C_s, and C_a. The $C1$ and $C2$ curves are due to the ZVS turn-ON constraint for Conditions I and II. If n and L are chosen along the curves $C1$ and $C2$ for conditions I and II, respectively, then the duty ratio required to achieve V_o is more than the d_{min}. Thus, the four plots do not show the curves due to the minimum duty constraint. $B1$ is

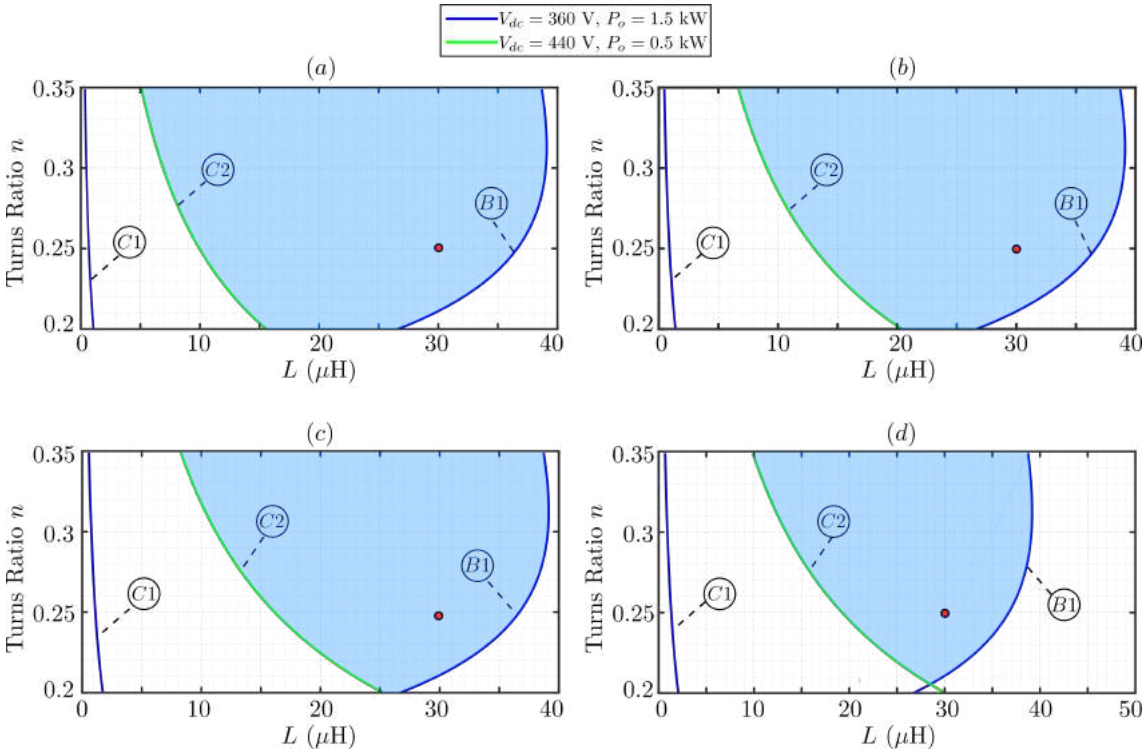


Fig. 3.7: n v/s L plots for the two extreme operating conditions. The four plots are for different external parasitic capacitances (*a*) $C_{ext} = 0$ pF, (*b*) $C_{ext} = 100$ pF, (*c*) $C_{ext} = 200$ pF, (*d*) $C_{ext} = 300$ pF.

the curve due to the maximum duty constraint for condition I. For condition II the curve due to d_{max} is obtained at larger values of L and thus is not visible in the plots.

Leakage inductance $L = 30\,\mu$H and the turns ratio $n = 0.25$ is chosen considering, C_{ext} added to C'_p, C'_s, and C'_a can vary from 0 to 300 pF. A smaller value of n is selected for the following reasons.

- It would result in lower conduction losses of the devices and magnetics in the primary.
- It would reduce the reverse breakdown voltage rating of the rectifier bridge diodes.
- Since $C_s = n^2(C'_s + C_{ext})$, a smaller n would reduce the peak of the snubber current given by $\frac{V_{dc}\sqrt{(C_a+C_s)}}{\sqrt{L}}$, reducing the conduction losses in the snubber.

Once n and L are determined, the junction temperature rise is re-checked for the primary devices not to exceed the maximum allowable temperature. Also, the blocking capability (V_b) of the secondary diodes is re-verified such that $nV_{dc,max}$ does not exceed the maximum limit. If the above conditions are not satisfied, the extraction of capacitances and Step 2 are followed using new devices.

3.5 Step 3: Dead-time selection

Dead time is defined as a short interval between the turn-OFF and turn-ON of the two complementary switches. It is introduced to prevent the accidental shorting of DC bus through the two switches. Moreover, its proper selection becomes even more crucial to achieve zero voltage switching in a PSFB converter. Section 2.2.2 discusses that the necessary dead time t_{dead} to achieve successful ZVS turn-ON is given by

$$\sqrt{LC_p}\sin^{-1}\left(\frac{V_{dc}\sqrt{C_p}}{nI_o\sqrt{L}}\right) < t_d < \sqrt{LC_p}\sin^{-1}\left(\frac{V_{dc}\sqrt{C_p}}{nI_o\sqrt{L}}\right) + \left[\left(\frac{nI_oL}{V_{dc}}\right)^2 - LC_p\right]^{1/2} \tag{3.14}$$

(3.14) shows that if the dead time is calculated for $V_{dc,max}$ and $I_{o,min}$, the converter will achieve ZVS turn-ON in all operating conditions. Thus, the dead time is chosen considering Condition II.

3.6 Step 4: Low Pass Filter Design

3.6.1 Filter Inductance (L_f)

PSFB being a buck-derived converter, the output inductor is designed as it is for a buck converter. During the active state, the voltage across the choke is $nV_{dc} - V_o$. Thus

$$L_f\left(\frac{\Delta I_o}{d_{eff}T_s/2}\right) = nV_{dc} - V_o$$

Where $d_{eff} = V_o/(nV_{dc})$ is the effective duty after subtracting all the duty losses in d.

$$L_f = \frac{\left(1 - \frac{V_o}{nV_{dc}}\right)V_o}{2f_s\Delta I_o} \tag{3.15}$$

To ensure the output current to be ripple free, the peak to peak ripple considered is 20% of the I_o at a minimum load of 0.5 kW. Thus, $\Delta I_o = 2A$ for an input voltage $V_{dc} = 440$ V, output voltage $V_o = 48$ V, $n = 0.25$, and switching frequency $f_s = 100$ kHz.

$$L_f = 65.52\,\mu\text{H} \tag{3.16}$$

3.6.2 Filter Capacitance (C_f)

The output capacitance filters out the high-frequency ripple in the output current. For $\Delta I_o = 2$ A and 1% per cent of ripple in the output voltage, i.e. $\Delta V_o = 0.48$ V

$$\begin{aligned} C_f &= \frac{\Delta I_o}{16f_s\Delta V_o} \\ &= 2.61\,\mu\text{F} \end{aligned} \tag{3.17}$$

3.7 Summary

The chapter presents a detailed design procedure for the PSFB converter and the proposed snubber. The analysis and converter gain expression obtained in Chapter 2 are used to achieve the design objectives like ZVS turn-ON and gain at all operating conditions, given the specifications of the converter. The chapter discusses determining transformer turns ratio n and leakage inductance L. This procedure requires the value of primary, secondary, and snubber parasitic capacitances. It also shows how the determination of n and L is affected by the value of these capacitances. Once the pair (L, n) is obtained, the chapter discusses the necessary dead time required to avoid partial soft switching. Finally, we design the converter's output filter.

Chapter4

Hardware Design

4.1 Introduction

In the previous chapter, we lay a design procedure for a PSFB with the proposed snubber utilising the converter gain expression derived in Chapter 2. We then determined the transformer turns ratio and the required main transformer leakage inductance to achieve ZVS turn ON and the desired output voltage in various operating conditions.

This chapter presents the hardware design required for developing a laboratory prototype. The first section of the chapter covers the main and the snubber transformer design by selecting an appropriate core and number of turns. The windings of the two transformers are constructed using Litz wires to reduce the HF conduction losses and increase the mechanical flexibility compared to single-strand conductors.
As discussed in Chapter 2, the magnitude of the rectifier bridge voltage overshoot depends on the ratio of the leakage inductances of the main and the snubber transformer; the chapter presents the winding layout with the leakage inductance calculations for the two transformers. The chapter also covers the heat sink selection for the different bridges and a brief discussion on the gate driver circuitry. Further, it shows a detailed design procedure for the output inductor with a toroidal iron core. Finally, the chapter gives a list of other major converter components.

4.2 Transformer Design

Operating at higher frequencies leads to a considerable reduction in the size of magnetics. However, [27] and [28] show that the transformer losses consisting of the core and the winding loss increase under non-sinusoidal and high-frequency excitations. The core loss comprises eddy current and hysteresis losses. A low conductivity ferrite material with a smaller hysteresis loop area can minimise the core loss. Therefore, N87 ferrite cores are used for transformer construction. The winding losses are due to skin and proximity effects in the high-frequency transformers. Interleaving techniques and the use of litz-wire help minimise the AC resistance by reducing the proximity effect in the windings. Thus, reducing the copper losses in the transformers. The two transformers are designed in the following steps:

- The magnetic core is chosen based on the area product method of transformer design.
- Number of primary and secondary turns are calculated.
- A detailed litz wire design is carried out.

- Transformer layout with interleaved windings is presented.
- The final step analytically calculates the leakage inductance of the transformers.

This section presents a detailed discussion about the above mentioned steps.

4.2.1 Core Selection

Fig 4.1 shows the transformer's primary voltage and magnetic flux density waveforms.

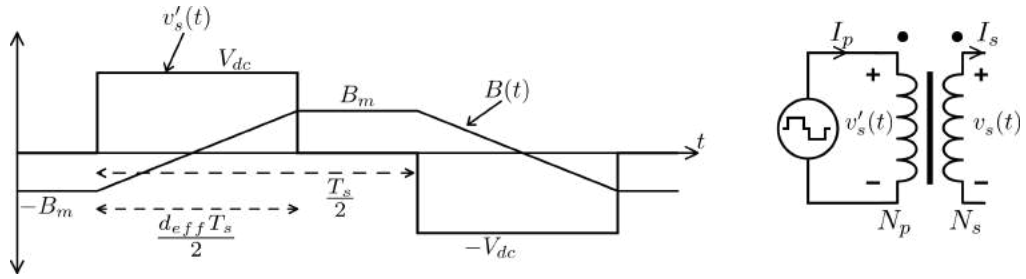


Fig. 4.1: Transformer's voltage and flux density waveforms.

Using Faraday's law,

$$\begin{aligned} V_{dc} &= N_p \frac{d\phi}{dt} \\ &= N_p A_c \frac{dB(t)}{dt} \end{aligned}$$

For a quasi square voltage waveform:

$$V_{dc} = \frac{4 N_p A_c B_m f_s}{d_{eff}} \tag{4.1}$$

The number of turns in the primary is N_p, and the magnetic flux flowing through the core is given by ϕ. B_m and A_c are the core's peak flux density and cross-sectional area, respectively. And the effective duty $d_{eff} = V_o/(nV_{dc})$.

To fit the primary and secondary windings in the transformer window,

$$K_w A_w = N_p w_p + N_s w_s \tag{4.2}$$

Where w_p and w_s are the wire cross-sectional areas of the primary and secondary winding. N_s is the total number of turns in secondary. A_w and K_w represent the window area and window utilisation factor, respectively.

Given the current density J, primary RMS current I_p, secondary RMS current I_s and

neglecting the magnetising current, (4.2) is given as

$$\begin{aligned} K_w A_w &= \frac{N_p I_p}{J} + \frac{N_s I_s}{J} \\ &= 2\frac{N_s I_s}{J} \end{aligned} \tag{4.3}$$

Therefore, the area product $A_w A_c$ is calculated using (4.1) and (4.3)

$$\begin{aligned} A_w A_c &= \frac{n d_{eff} V_{dc} I_s}{2 B_m f_s K_w J} \\ &= \frac{V_o I_s}{2 B_m f_s K_w J} \end{aligned}$$

Where n is the secondary to primary turns ratio.

$$A_w A_c = \frac{P_o'}{2 B_m f_s K_w J} \tag{4.4}$$

I_s approximately equals the average output current I_o for the main transformer. The transformer is designed for an output power of $P_o = 2\,\text{kW}$. Therefore, $P_o' = P_o$ for the main transformer. It is assumed that snubber transfers 25% of the rated output power. Thus snubber transformer is designed for $P_o' = 0.5\,\text{kW}$. Table 4.1 contains the parameters required to calculate respective area products.

Cores with area product greater than the mentioned in Table 4.1 and sufficient to fit the windings are chosen. **E 65/32/27 and ETD 59/39/22 are the cores used for the main and snubber transformers.**

Table 4.1: Core selection parameters of the transformers.

	Main Transformer	Snubber Transformer
P_o'	2 kW	0.5 kW
B_m	0.1 T	0.1 T
f_s	100 kHz	100 kHz
K_w	0.3	0.3
J	$4\,\text{A mm}^{-2}$	$4\,\text{A mm}^{-2}$
Computed $A_w A_c$	$8.334\,\text{cm}^4$	$2.1\,\text{cm}^4$

4.2.2 Primary and Secondary Turns

The total number of turns in the primary for the two transformers is calculated using (4.5).

$$\begin{aligned} N_p &= \frac{V_{dc} d_{eff}}{4 A_c B_m f_s} \\ &= \frac{V_o}{4 n A_c B_m f_s} \end{aligned} \tag{4.5}$$

The secondary turns for the transformer are calculated as expressed as below.

$$N_s = nN_p$$

Table 4.2 comprises the winding turns of the two transformers, given that $B_m = 0.1\,\mathrm{T}$, $n = 0.25$, $V_o = 48\,\mathrm{V}$, and $f_s = 100\,\mathrm{kHz}$.

Table 4.2: Primary and secondary turns of the two transformers.

	Main Transformer	Snubber Transformer
Core	E 65/32/27	ETD 59/31/22
A_c	$529\,\mathrm{mm}^2$	$368\,\mathrm{mm}^2$
N_p	12	16
N_s	3	4

4.2.3 Litz Wire Design

The following steps summarise the litz wire design procedure.

Calculate the Strand Diameter:
The diameter d_s of the single strand is chosen as half of the skin depth δ calculated as follows.

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_o}} \tag{4.6}$$

Where f is the frequency of the sinusoidal current in the winding, ρ is the resistivity of the conductor, and μ_o is the permeability of free space. However, [29] shows that for a non-sinusoidal current, (4.6) can be used by replacing f with f_{eff}, i.e. an effective sinusoidal frequency calculated as expressed in (4.7).

$$f_{eff} = f_s \sqrt{\frac{6}{\Delta_i(3 - 4\Delta_i)}} \tag{4.7}$$

Where Δ_i is the ratio of transition time T_r to total switching time period T_s of the current flowing through the transformer as shown in the Fig 4.2.

$$\begin{aligned} \Delta_i &= \frac{T_r}{T_s} \\ &= f_s \frac{2nI_oL}{V_{dc}} \end{aligned} \tag{4.8}$$

Substituting (4.8) in (4.7) we get, $f_{eff} = 128.76\,\mathrm{kHz}$. Using (4.6), $f = f_{eff}$, $\mu_o = 12.566 \times 10^{-7}\,\mathrm{H\,m^{-1}}$, and $\rho_{copper} = 1.78 \times 10^{-8}\,\Omega\,\mathrm{m}$, the calculated skin depth is $\delta = 0.198\,\mathrm{mm}$. The selected strand diameter is half of the skin depth. Thus, $d_s = 0.1\,\mathrm{mm}$.

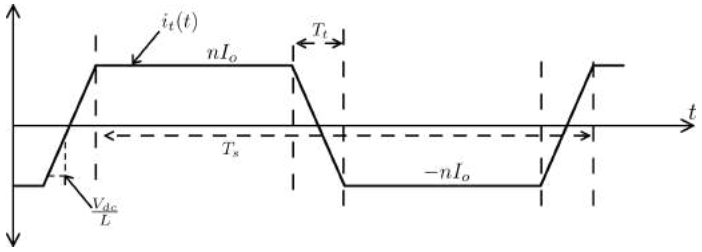


Fig. 4.2: Approximate current waveform flowing through the main transformer.

Calculate Total Number of Strands:
Once we determine the diameter of a single strand, we can find the total number of strands S_T per turn of the primary and secondary windings of the two transformers. S_T is computed such that the current density does not cross the limit of $J = 4.2\,\mathrm{A\,mm^{-2}}$.

$$S_T = \frac{4I_w}{J\pi d_s^2} \tag{4.9}$$

I_w is the current flowing in the respective winding for which the total number of strands is being calculated. Table 4.3 contains S_T, calculated for each winding of the two transformers.

Determine the Level of Bundling:
To reduce the bundle level skin effect problem, the total number of strands are divided using a multi-level bundling technique [29] [30] as shown in Fig 4.3.

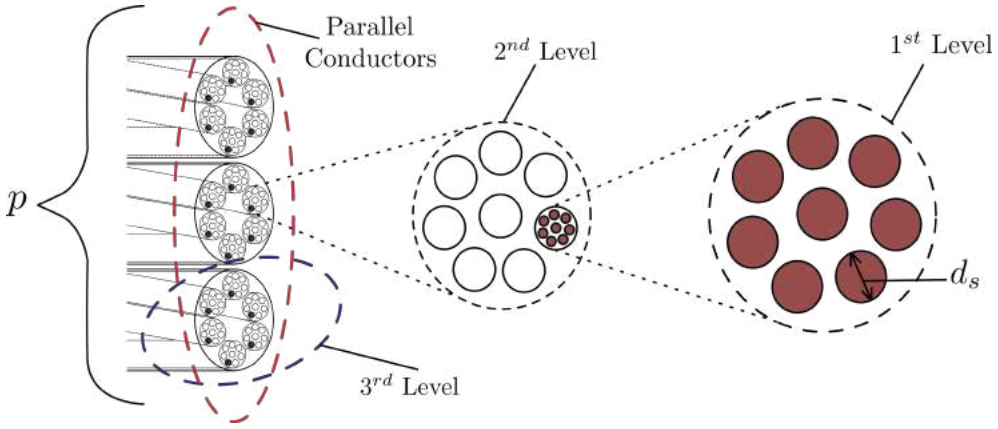


Fig. 4.3: General multi-level bundling structure of a litz wire.

The first level of twisting has no more than s_{max} number of strands per twist.

$$\begin{aligned} s_{max} &= 4\left(\frac{\delta}{d_s}\right)^2 \\ &\approx 16 \end{aligned} \tag{4.10}$$

Rest incremental twisting levels are ≤ 5 strands per twist.

The bundling structure is expressed as $(a \times b \times c)p$. Where $a = s_{max}$, b, and c are the number of strands in the 1^{st}, 2^{nd}, and 3^{rd} level, respectively. p is the number of parallel conductors in a single turn. Thus, these are chosen such that $S_T = (a \times b \times c) \times p$. Table 4.3 consists of the bundling structure of the primary and secondary windings of the main and snubber transformers.

Table 4.3: Litz wire structure of the four windings.

	Main Transformer Winding		Snubber Transformer Winding	
	Primary	Secondary	Primary	Secondary
S_T	288	1200	128	432
a	16	16	16	16
b	3	5	2	3
c	3	5	-	3
p	2	3	4	3

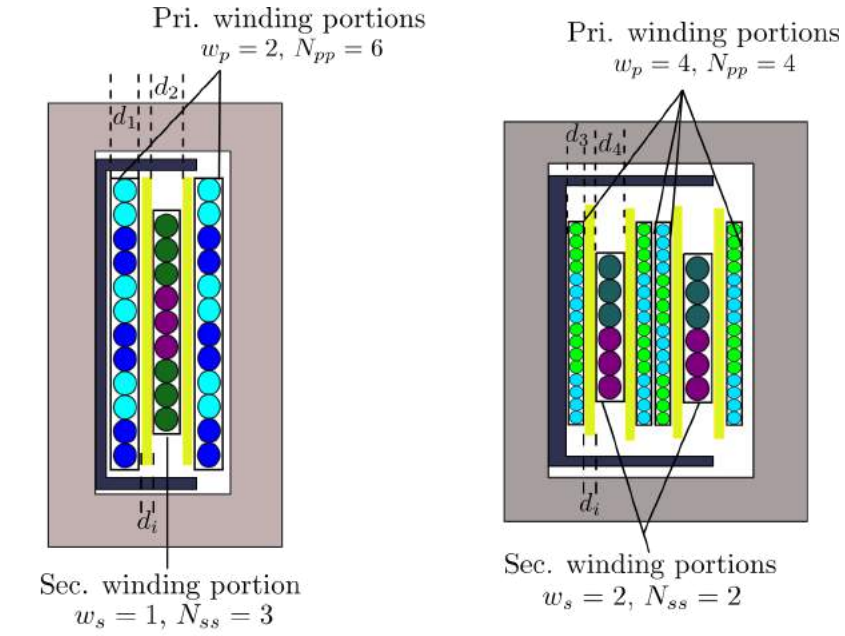
4.2.4 Transformer Winding Layout

AC excitation in a transformer produces an alternating magnetic flux. This flux flows through a magnetic core and links the transformer's secondary winding, producing an EMF in the secondary. However, not all flux links the secondary, causing imperfect coupling. [31] shows that interleaving is a common strategy to reduce this leakage flux. It is a technique in which the primary and the secondary windings are divided into several winding portions. It is desired to minimise the leakage inductances of the two transformers. The additional inductance necessary for the ZVS turn-on of the converter is achieved through an external inductor L_{ext}.
The number of turns in the primary and secondary of the transformer are represented by N_p and N_s, respectively. Let N_{pp} and N_{ss} be the number of turns in a single winding portion. Then the total number of such segments for primary and secondary can be given by w_p and w_s.

$$N_{pp} = \frac{N_p}{w_p}$$

$$N_{ss} = \frac{N_s}{w_s}$$

The winding data and layout for the main and the snubber transformer is shown in Table 4.4 and Fig 4.4, respectively.



(a) Main Transformer (b) Snubber Transformer

Fig. 4.4: Winding layout of the two transformers

Table 4.4: Winding data for the two transformers.

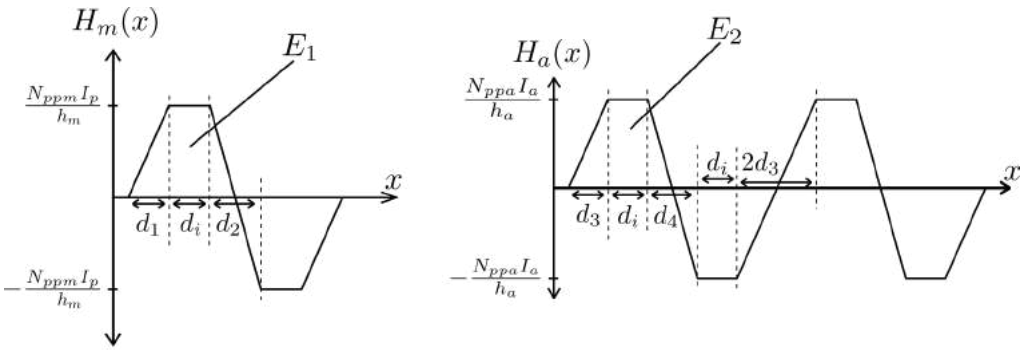
	Primary			Secondary		
	N_p	N_{pp}	w_p	N_s	N_{ss}	w_s
Main Transformer	12	6	2	3	3	1
Snubber Transformer	16	4	4	4	2	2

4.2.5 Analytical calculation of Leakage Inductance

The voltage overshoots due to resonance between the leakage inductance and diode bridge capacitance are dependent on the ratio of L_a and L, where L is $L_{lk}+L_{ext}$. Thus, it becomes essential to calculate the leakage inductances of the two transformers analytically. [32] and [33] show that we can estimate the leakage inductance by calculating the leakage energy stored in the windings and insulation. [34] shows that using the stored energy method, the error in calculating leakage inductance is around 5-15%. The stored energy E in a single winding portion and insulation is calculated using (4.11).

$$E = \frac{1}{2}\mu_o(MLT)h\int[H(x)^2]dx \tag{4.11}$$

Where $H(x)$ is spatial function of MMF and MLT is the mean length turn of the winding. The average height of the primary and secondary windings is given by h and permeability of free space is μ_o. **Main Transformer Leakage Inductance L_{lk}:**



(a) Main Transformer (b) Snubber Transformer

Fig. 4.5: MMF diagrams of the two transformer windings. The MMF diagrams are symmetrical and have been derived using the winding layout in Fig 4.4.

Fig 4.5(a) shows the MMF diagram of the main transformer. The diagram has been derived using the winding layout in Fig 4.4(a). The width of the primary and secondary winding portion is given by $d_1 = 3.6\,\text{mm}$ and $d_2 = 5\,\text{mm}$, respectively. Each of these portions is separated by an insulation layer of thickness $d_i = 1\,\text{mm}$. The height h_m of the winding is the average height of the primary and secondary windings. $MLT = 201\,\text{mm}$ is the mean length turn of the windings. Using (4.11) and $H(x) = H_m(x)$ in Fig 4.5(a), the total leakage inductance of the main transformer, referred to primary can be calculated as

$$\frac{1}{2}L_{lk}I_p^2 = \frac{1}{2}\mu_o(MLT)h_m\int[H_m(x)^2]dx$$

$$L_{lk} = \frac{\mu_o(MLT)h_m}{I_p^2}\int[H_m(x)^2]dx \tag{4.12}$$

Where $N_{ppm} = 6$ is the number of turns in a single portion of the primary winding and I_p is the primary current of the main transformer. Thus, using (4.12) $L_{lk} = 3.032\,\mu\text{H}$.

Snubber Transformer Leakage Inductance L_a:

Fig 4.5(b) shows the MMF diagram of the snubber transformer. The diagram has been derived using the winding layout in Fig 4.4(b). The width of the primary and secondary winding portion is given by $d_3 = 2.1\,\text{mm}$ and $d_4 = 4\,\text{mm}$, respectively. Each of these portions is separated by an insulation layer of thickness $d_i = 1\,\text{mm}$. The height $h_m = 19\,\text{mm}$ of the winding is the average height of the primary and secondary windings. $MLT = 150\,\text{mm}$ is the mean length turn of the windings. Using (4.11) and $H(x) = H_a(x)$ in Fig 4.5(b), the total leakage inductance of the snubber transformer, referred to primary can be calculated as

$$\frac{1}{2}L_aI_a^2 = \frac{1}{2}\mu_o(MLT)h_a\int[H_a(x)^2]dx$$

$$L_a = \frac{\mu_o (MLT) h_a}{I_a^2} \int [H_a(x)^2] dx \tag{4.13}$$

Where $N_{ppm} = 4$ is the number of turns in a single portion of the primary winding and I_a is the primary current of the snubber transformer. Thus, using (4.13) $L_a = 2.1\,\mu H$.

4.3 Heat Sink Selection

Device and thermal paste datasheets provide the junction to case and case to sink thermal resistances, respectively. These are used to determine the junction temperature rise T_j of the devices. The devices of the inverter and rectifier bridges are selected in Chapter 2 such

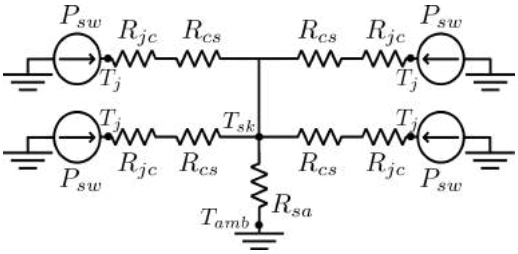


Fig. 4.6: Steady state thermal model of the bridges.

that the T_j must not exceed 75% of the rated junction temperature $T_{j,max}$, considering that the heat sink temperature T_{sk} is at $80°C$.

The layout configuration of the switches on the heat sink is such that all the four devices are placed back to back, as shown in Fig 4.8. +12 V BLDC fans are employed to achieve forced cooling.
Assuming $T_{sk} = 80°C$ and ambient temperature $T_{amb} = 30°C$, we calculate the total power loss that can flow through the heat sinks while maintaining the T_{sk} at $80°C$. Fig 4.6 shows the steady state thermal model of the bridges. Junction to case thermal resistances R_{jc} and case to sink thermal resistance R_{cs} can be extracted from the device and thermal paste datasheets, respectively. The heat sink datasheet of Wakefield-Vette omniKlip provides the graphs of thermal resistances per device vs. the fan flow rate. Choosing a fan with

Table 4.5: Thermal Components for the two bridges.

	Inverter	Secondary Diode Bridge
P_{sw}	10 W	25 W
Heat Sink	OMNI-UNI-32-58	OMNI-UNI-41-75
Fan Part No.	109P0412K3023	PMD1206PTVX-A.U.GN
R'_{sa} (°C/W)	5	2
R_{sa} (°C/W)	1.75	1

a suitable flow rate, such that the corresponding thermal resistance R_{sa} is less than R'_{sa} calculated as shown in 4.14.

$$R'_{sa} = \frac{T_{sk} - T_{amb}}{P_{sw}} \tag{4.14}$$

Where P_{sw} is the total power loss of a single device (MOSFET for inverter and Schottky diode for rectifier bridges). Table 4.5 consists of the heat sinks for the two bridges, DC fans used for forced cooling and corresponding thermal resistance R_{sa}.

4.4 Gate Driver Circuitry

Fig 4.7 shows the gate driver schematic used for driving the inverter switches. The positioning of the gate driver circuit is kept very close to the MOSFET terminals, as shown in Fig 4.8. Analog Devices's gate driver ADuM4135 is used to drive the inverter bridge devices. It is a single-channel gate driver IC that includes a Miller clamp to provide robust turn-off with a single supply rail when gate voltage drops below 2 V. An integrated desat-

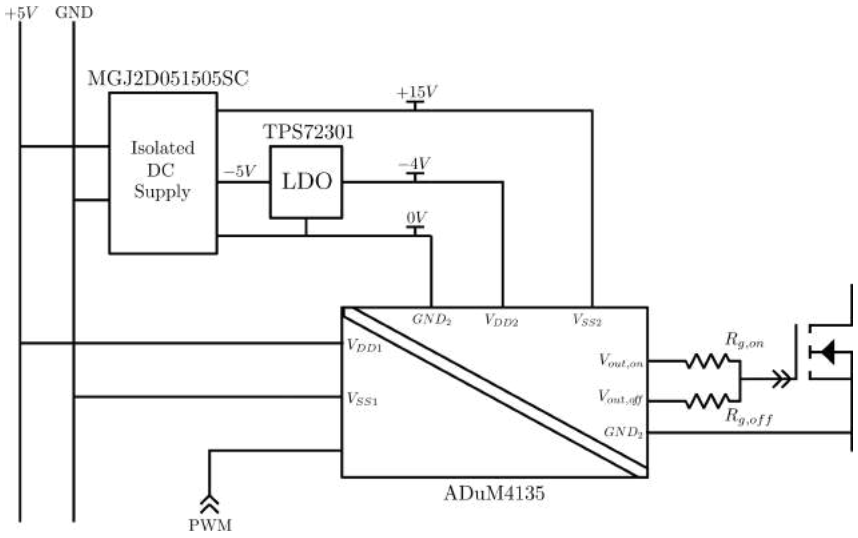


Fig. 4.7: Gate driver circuit

uration detection circuit provides high voltage short circuit protection. It also has input and output under-voltage lockout. All voltages are referenced to V_{SS1} on the low voltage side while to GND_2 on the high voltage side. Input supply volatge is +5 V. Positive and negative supply from secondary are +15 V and −4 V. The driver has split outputs, which enable to use different gate resistors for turn-on and turn-off. The designed gate driver circuit has a provision for manual and automatic reset of the fault. The converter is operated in open loop using TMS320F28379D micro-controller.

4.5 Output Inductor

PSFB is buck derived converter operating in continuous conduction mode, i.e. the peak to peak ripple current ΔI_o is much smaller than the load current I_o. The filter inductor sizing depends on the peak $I_{pk} = I_o + \frac{\Delta I_o}{2}$ and the RMS $I_{o,rms}$ of the output current. The peak of the current decides the maximum magnetic flux density B_m and energy the inductor would be storing. This maximum flux density should be less than the flux density B_{sat} at which the core saturates. While the RMS value of the current determines the size of the wires to wound the coil.

The maximum flux linkage is expressed as in (4.15).

$$L_f I_{pk} = N A_c B_m \tag{4.15}$$

Where L_f is the output inductance and N is the number of turns. The cross-sectional area of the core is represented by A_c.
Given the current density J, the required wire cross-section a_w can be calculated as follows.

$$\begin{aligned} a_w &= \frac{I_{o,rms}}{J} \\ &= \frac{I_{pk}}{JK_p} \end{aligned} \tag{4.16}$$

Where K_p is the peak factor of the output current. Thus, given the window utilisation factor of K_w, the winding fits the core window if

$$\begin{aligned} N a_w &= K_w A_w \\ I_{pk} &= \frac{J K_p K_w A_w}{N} \end{aligned} \tag{4.17}$$

E_i is the maximum magnetic energy stored in the inductor.

$$E_i = \frac{1}{2} L_f I_{pk}^2 \tag{4.18}$$

Using (4.15) and (4.17), (4.18) can be written as

$$E_i = \frac{1}{2} \left(N A_c B_m \right) \left(\frac{J K_p K_w A_w}{N} \right)$$

Therefore,

$$A_c A_w = \frac{2 E_i}{K_w K_p B_m J} \tag{4.19}$$

The choke is designed for an average output power of 2 kW and 20% of ripple in the output current at a load of 0.5 kW. Then, for $I_o = 42\,\text{A}$, $\Delta I_o = 2\,\text{A}$, $I_{pk} = 43\,\text{A}$, $L_f = 65.52\,\mu\text{H}$, $K_p \approx 1$, $K_w = 0.6$, $J = 4\,\text{A mm}^{-2}$, and $B_m = 0.2\,\text{T}$, we get $A_w A_c = 25.238\,\text{cm}^4$.

A core with an area product of more than the calculated is suitable for the choke design. Therefore, MAGNETICS's powdered iron core 0077617*A*7 is chosen for the filter choke. It is a toroidal core with a distributed air gap to prevent it from going into saturation and storing the magnetic energy. The core has a relative permeability of 60 with permeance λ of 189 nH/Turn^2. The number of turns required are

$$\begin{aligned} N &= \sqrt{\lambda L_f} \\ &\approx 19 \end{aligned} \tag{4.20}$$

To keep the current density around 4 A mm^{-2}, five copper wires (SWG 16) of diameter 1.626 mm are used to make 19 turns.

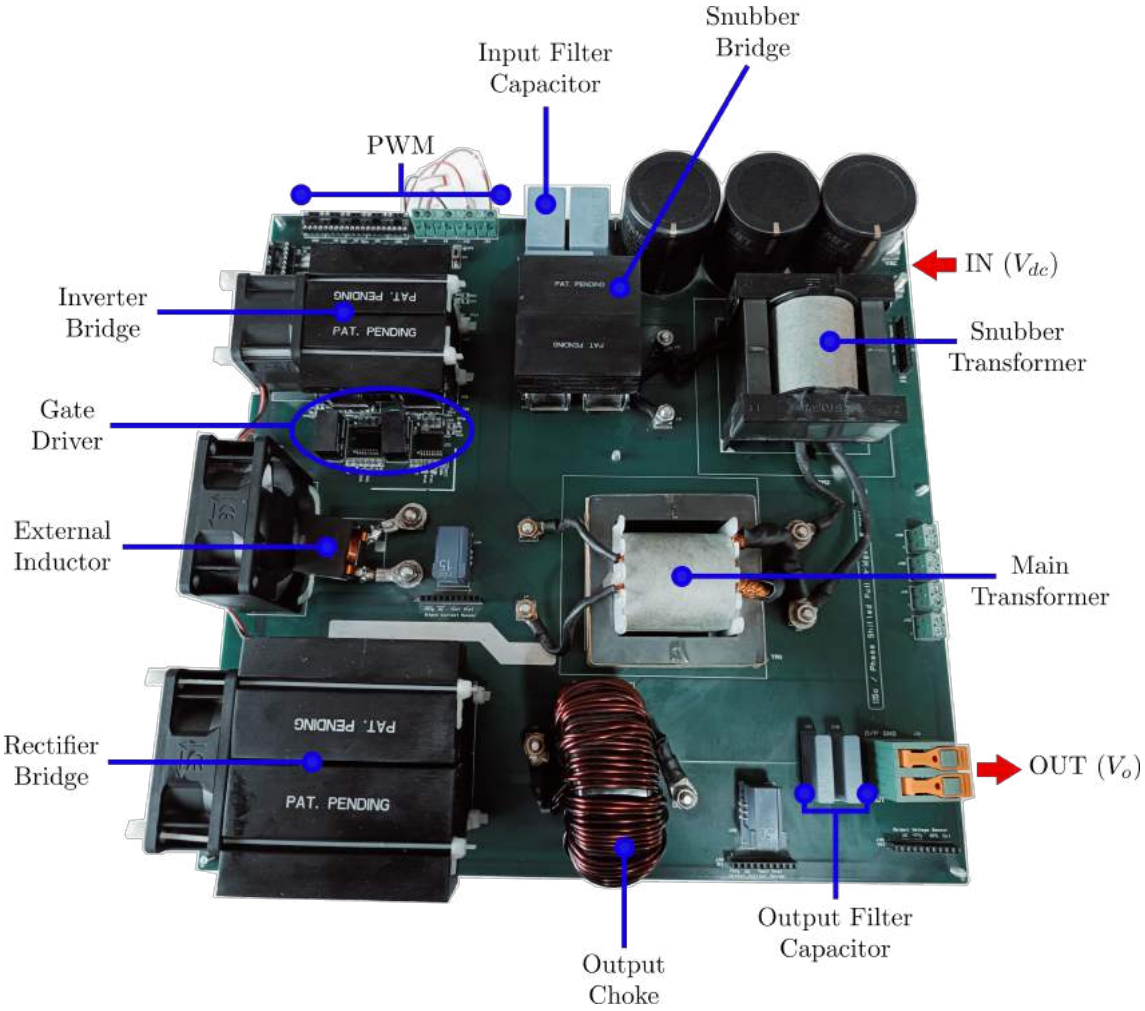


Fig. 4.8: PSFB hardware setup with the proposed snubber.

Table 4.6: Other major converter components.

Component	Part No.	Remarks
Inverter Bridge Devices	C3M0120065K	The device is chosen as per Section 3.3.1. It is a 650 V, 22 A SiC MOSFET with a maximum junction temperature of 175°C. Wolfspeed manufactured TO 247-4 package with a Kelvin source terminal gives better switching performance.
Sec. Rectifier Devices	DSSK60-02AR	The IXYS manufactured 200 V, 2 × 30 A, TO-247 package is a Si Schottky diode selected as per Section 3.3.2. The maximum junction temperature is 175°C. The device includes two diodes in a common cathode configuration.
Snubber Bridge Devices	E3D20065D	The 650 V SiC snubber Schottky diode is chosen in Section 3.3.3. It is rated for a maximum reverse voltage of 650 V and 20 A of current.
External Inductor	B82559A0303A024	The main transformer's leakage inductance after interleaving is insufficient to achieve 30 µH thus, an external inductor B82559A0303A024 of 30 µH with 10 A of saturation current at 100°C is added.
Input DC link Capacitor	B32774P6475K000	Each EPCOS B32774P6475K000 is a 4.7 µF film capacitor rated for 630 V. Three of these capacitors are connected in parallel to produce a combined capacitance of 14.1 µF sufficient to supply the entire AC component of the input current.
Output Filter Capacitor	B32523Q1475K	The output filter capacitance is calculated as per Section 3.6.2. EPCOS B32523Q1475K is a 4.7 µF and 100 V film capacitor with 10% tolerance. Two of these capacitors are connected in parallel to obtain a combined capacitance of 9.4 µF.

4.6 Other Converter Components

Table 4.6 comprises some major converter components. A provision for accepting both analog and optical PWM signals is available on the PCB.

Fig 4.8 shows the hardware setup of the converter and placement of the different hardware components on the board. The dimensions of the entire converter are 310 mm $\times$ 300 mm.

4.7 Summary

The hardware prototype to be built is a 400($\pm$10%) V to 48 V PSFB delivering an output power of 0.5-1.5 kW. The chapter presents the hardware design of the different converter components. A detailed design of the two HF Litz wire transformers is presented. The interleaving technique is used to reduce the leakage inductance of the two transformers. Finally, the chapter briefly discusses the selection of heat sinks, gate driver circuits and filter inductor design.

Chapter5

Experimental Verification

5.1 Introduction

A detailed design procedure and hardware development are discussed in Chapters 3 and 4. A 400(±10%) V/48 V, 1.5 kW PSFB hardware prototype was developed and various laboratory experiments are conducted to verify the following.

- The effectiveness of the proposed snubber in reducing the voltage overshoots across the diode bridge rectifier.
- The accuracy of the PSFB analysis and the derived closed-form expressions for the converter state variables.
- The design objectives of achieving desired converter gain and ZVS turn ON for all inverter switches at all operating conditions.

The chapter starts with the estimation of different converter parameters. Frequency Response Analysis (FRA) and Waveform Estimation (WE) are the two methods used for it. Parameters like inductances and their parasitic capacitances of the magnetic components are estimated using FRA. For instance, the two transformers' open and short circuit input impedances give the leakage and magnetising inductances. WE method uses the converter state variable waveforms to evaluate the circuit parameters mentioned above and the different dominant circuit parasitic capacitances. These parameters are then used to verify the mentioned objectives.

The chapter presents the experimental results and compares them with the analytical calculations to show the proposed snubber's effectiveness and analysis. The chapter uses the closed-form expressions obtained in Chapter 2 to plot the state variable waveforms and compares them with the measured converter voltages and currents. A detailed comparison of experimental and analytically calculated duty ratios for different operating conditions is presented. Further, the experimental results validate the ZVS turn ON of the inverter switches. At last, it submits the efficiency results of the converter and the loss distribution of the converter components.

5.2 Parameters Estimation

This section presents different parameter estimation methodologies. Parameters related to magnetics like transformer leakage and magnetising inductance are measured using Frequency Response Analysis (FRA). Further, we can determine circuit parameters experimentally through converter state variable waveforms. Let's call this method as Waveform Estimation (WE).

5.2.1 Parameter Estimation Using FRA

Using PSM3750, frequency response analysis was conducted to measure the different parameters of the two high-frequency transformers and the added external inductance. Although Bode-magnitude plots of the two transformers and the inductor provide the inductances mentioned and interwinding capacitances, it doesn't give any information about the overall circuit parasitic capacitances (C_p, C_s, and C_a), discussed in the last two chapters. These parameters are estimated in the next section using converter state variables.

Transformer Characterisation

Fig 5.1 shows the high-frequency (HF) transformer model [35] considered for FRA tests. It is also assumed that the core loss component of the exciting current is negligible. R_p and

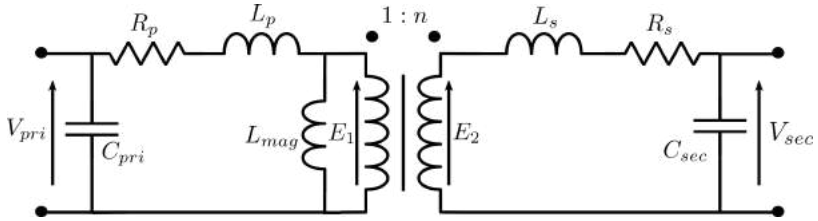


Fig. 5.1: High-Frequency Transformer Model

L_p represent primary winding resistance and leakage inductance of the primary winding. On the other hand, L_s and R_s denote the secondary winding parameters. Also, C_{pri} and C_{sec} are primary and secondary winding capacitances, respectively. While L_{mag} is the magnetising inductance referred to transformer's primary.

I. Open Circuit Test

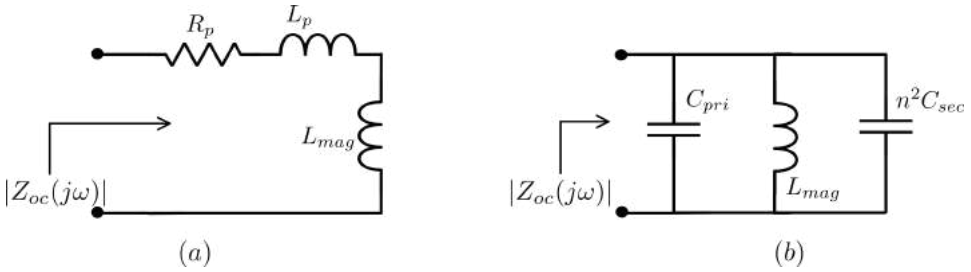
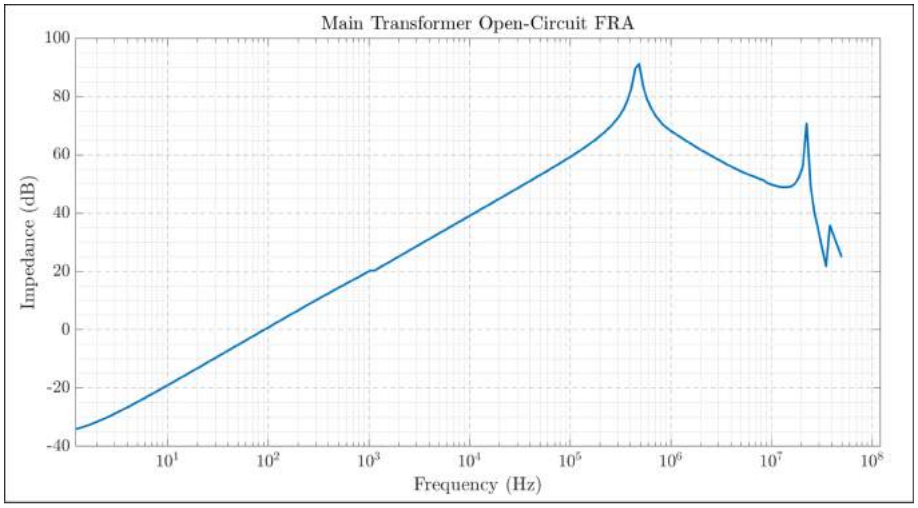
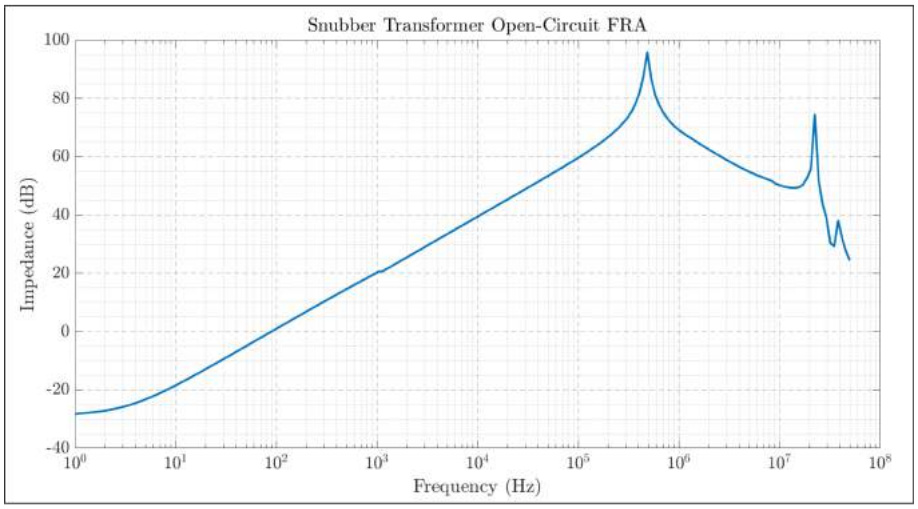


Fig. 5.2: Approximate equivalent circuit with open-circuited LV windings. (a) At low frequencies, i.e. the constant slope region in Bode-magnitude plot. (b) At high frequencies, i.e. around first resonant frequency.

The low-voltage (LV) side of the transformer is kept open to measure the high-voltage (HV) input impedance $Z_{oc}(j\omega)$. Fig 5.2 shows the equivalent circuits for the input impedance measurement when the transformer's LV secondary is open-circuited. The parasitic capac-



(a)



(b)

Fig. 5.3: HV input impedance Bode-magnitude plot with open-circuited LV terminals. (a) Main transformer impedance. (b) Snubber transformer impedance.

itances do not influence the measurements in the lower frequency range, i.e. the constant slope region in Fig 5.3. Thus, at low frequencies

$$\begin{aligned} Z_{oc}(j\omega) &= R_p + j\omega(L_p + L_{mag}) \\ &\approx j\omega L_{mag} \end{aligned} \tag{5.1}$$

Therefore, an asymptote drawn in the frequency range where impedance magnitude has a near constant slope gives the magnetising inductance L_{mag}.

The impedance of leakage inductances and the winding resistances is much smaller than the impedances due to winding capacitances and magnetizing inductance at higher frequencies; thus, the series components R_p, R_s, L_p, and L_s can be neglected at high frequencies. Therefore, at higher frequencies the input impedance can be expressed as

$$Z_{oc}(j\omega) = j\omega L_{mag} || \frac{1}{j\omega(C_{pri} + n^2 C_{sec})} \tag{5.2}$$

The first resonant peak frequency f_{r1} gives the parallel combination of winding capacitances as shown in (5.3).

$$C_{pri} + n^2 C_{sec} = \frac{1}{(2\pi f_{r1})^2 L_{mag}} \tag{5.3}$$

Table 5.1 is filled using (5.1), (5.3) and Bode-magnitude plots shown in Fig 5.3.

Table 5.1: Transformer parameters obtained from open-circuit test.

	Main Transformer	Snubber Transformer
L_{mag}	1.44 mH	1.511 mH
f_{r1}	486.9 kHz	486.9 kHz
$C_{pri} + n^2 C_{sec}$	74.2 pF	70.71 pF

II. Short Circuit Test

The HV side input impedance is measured shorting the LV side of the transformer as shown by the equivalent circuit in Fig 5.4. Therefore, the low frequency impedance with

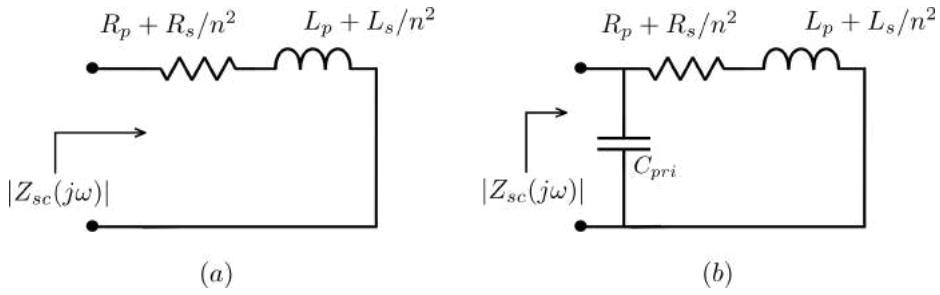
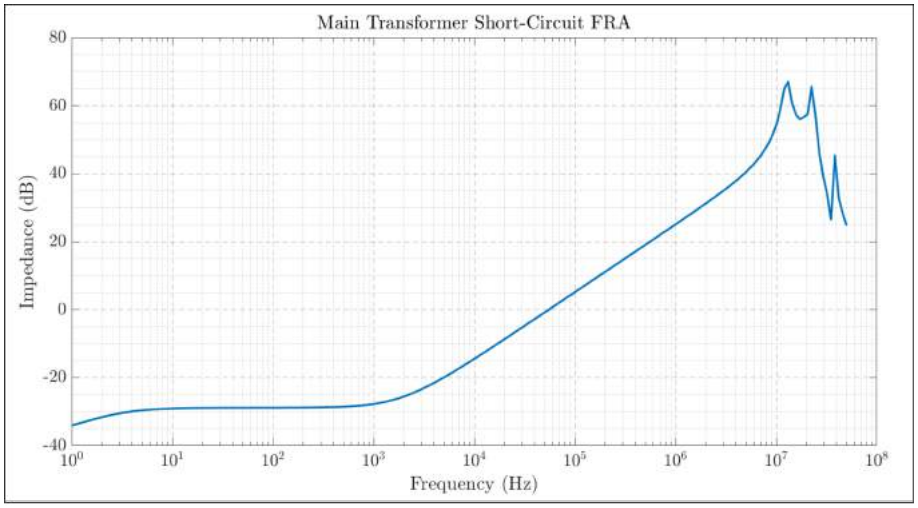


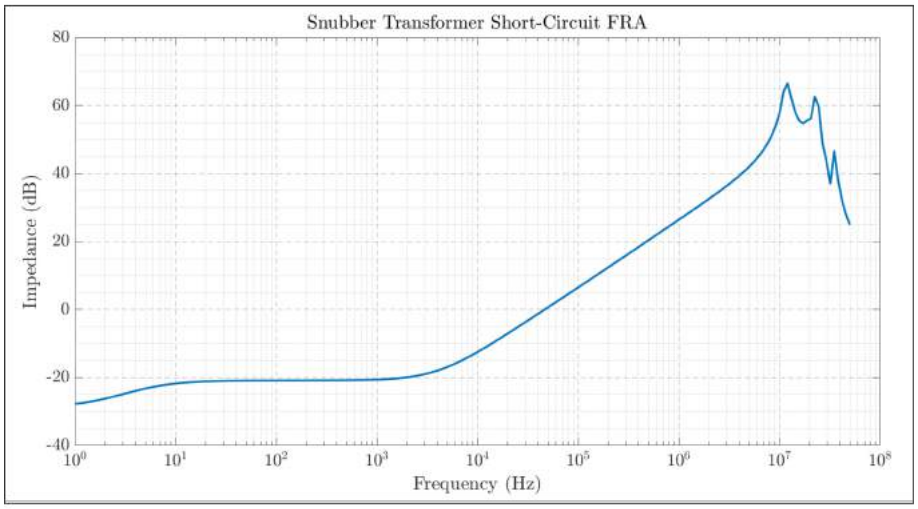
Fig. 5.4: Equivalent circuit with short-circuited LV windings. (a) At low frequencies, i.e. the constant slope region in Bode-magnitude plot. (b) At high frequencies, i.e. around first resonant frequency.

LV terminals shorted is expressed as follows.

$$Z_{sc} = \left(R_p + \frac{R_s}{n^2}\right) + j\omega\left(L_p + \frac{L_s}{n^2}\right) \tag{5.4}$$



(a)



(b)

Fig. 5.5: HV input impedance Bode-magnitude plot with shorted LV terminals. (a) Main transformer impedance. (b) Snubber transformer impedance.

The asymptote drawn in the low frequency and constant magnitude region of Fig 5.5 gives the total DC winding resistance referred to primary, $R_p + R_s/n^2$. The leakage inductance referred to primary is determined by using the first corner frequency f_{c1} as follows.

$$L_p + \frac{L_s}{n^2} = \frac{R_p + R_s/n^2}{2\pi f_{c1}} \tag{5.5}$$

The short-circuit input impedance at higher frequencies is given as

$$Z_{sc}(j\omega) = \frac{1}{j\omega C_{pri}} \,||\, j\omega \left(R_p + L_p + \frac{R_s + L_s}{n^2} \right) \tag{5.6}$$

The first resonant peak frequency f_{r2} gives the primary winding capacitance C_{pri} as expressed in (5.7).

$$C_{pri} = \frac{1}{(2\pi f_{r2})^2 (L_p + L_s/n^2)} \tag{5.7}$$

Table 5.2 is filled using (5.5), (5.7), and Bode-magnitude plots shown in Fig 5.5.

Table 5.2: Transformer parameters obtained from short-circuit test.

	Main Transformer	Snubber Transformer
$R_p + R_s/n^2$	36.1 mΩ	89.13 mΩ
f_{c1}	1.75 kHz	4.82 kHz
$L_p + L_s/n^2$	3.3 µH	2.94 µH
f_{r2}	13.15 MHz	12.03 MHz
C_{pri}	43.1 pF	59.53 pF

External Inductor (L_{ext}) Characterisation

The leakage inductance of the main transformer alone would be insufficient to achieve a series inductance of 30 µH; thus, an external inductor is added in series with the leakage inductance of the main transformer. EPCOS's B82559A0303A024 is a 30 µH inductor measured at 100 kHz, with a self-resonant frequency > 2 MHz. Fig 5.6 shows the considered high-frequency model of the inductor. Capacitance $C_{L_{ext}}$ can be neglected in LF modelling

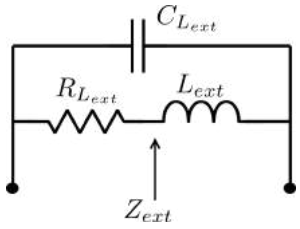


Fig. 5.6: High-frequency inductor model

of inductor. Therefore, the LF input impedance of the inductor is

$$Z_{ext} = R_{ext} + j\omega L_{ext} \tag{5.8}$$

The DC resistance measured is

$$R_{L_{ext}} = 4.1\,\text{m}\Omega \tag{5.9}$$

Fig 5.7 shows the Bode-magnitude plot of the external inductor to verify the inductance. The first corner frequency is observed at 20 Hz, which gives

$$L_{ext} = 32.6\,\mu\text{H} \tag{5.10}$$

The HF input impedance of the inductor is expressed as

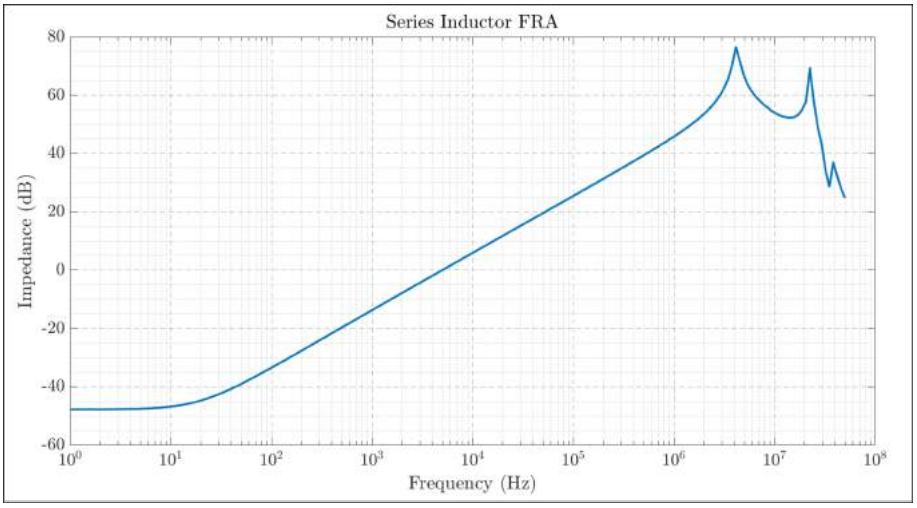


Fig. 5.7: Series inductor frequency response.

$$Z_{ext} = \frac{1}{j\omega C_{ext}} || (R_{ext} + j\omega L_{ext}) \tag{5.11}$$

The first resonance is observed at frequency of 4.13 MHz. Thus,

$$C_{L_{ext}} = 45.55\,\text{pF} \tag{5.12}$$

Therefore, the total series inductance L to achieve ZVS turn ON is the sum of the measured main transformer leakage inductance L_{lk} and L_{ext}, which is 35.9 µH. The snubber transformer's leakage inductance is $L_a = 2.94\,\mu\text{H}$.

5.2.2 Parameter Estimation Using WE

With the detailed PSFB analysis in Chapter 2, we obtained closed-form expressions for the state variables in terms of different circuit parameters, like leakage inductances and parasitic capacitances. Conversely, these circuit parameters can be estimated using the same measured state variables.

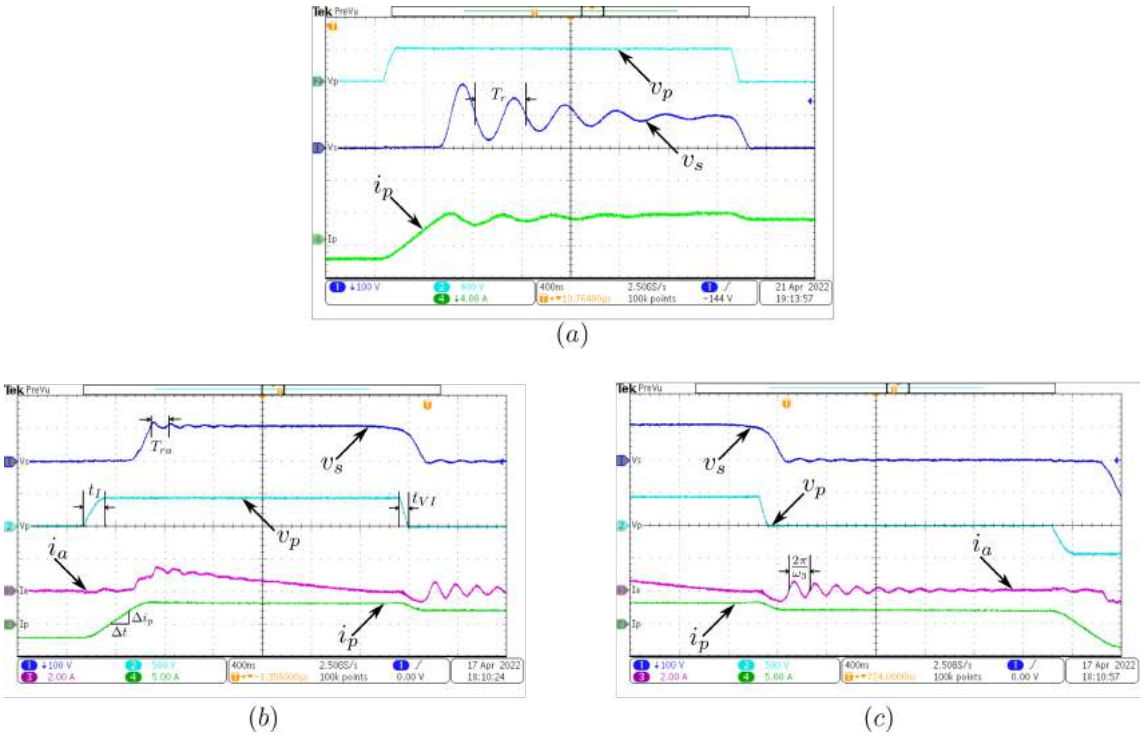
Series Inductance (L)

Equations (2.11) and (2.14) show the linear rise of the primary current i_p during the current commutation modes, i.e. mode II and III. The rate of change of i_p shown in Fig

5.8(b) is given by

$$\frac{\Delta ip}{\Delta t} = \frac{V_{dc}}{L} \tag{5.13}$$

For $11.342\,\mathrm{A\,\mu s^{-1}}$ of current rise and $V_{dc} = 400\,\mathrm{V}$, $L = 35.267\,\mu\mathrm{H}$.



(a) (b) (c)

Fig. 5.8: Converter state variable waveforms at $V_{dc} = 400\,\mathrm{V}$ and $P_o = 0.5\,\mathrm{kW}$ for parameter estimation. (a) Without snubber. (b),(c) With proposed snubber

Primary Referred Secondary Capacitance (C_s)

The converter is operated without the snubber to estimate the rectifier bridge diode capacitances. The frequency of the high voltage oscillations in the transformer's secondary voltage v_s in the active mode, as shown in Fig 5.8(a), gives the required information. The secondary voltage v_s in (1.4) rings with a resonant frequency of $f_r = \frac{1}{\sqrt{LC_s}}$, where $C_s = 2n^2C_d$. C_d is the junction capacitance of a diode of the rectifier bridge. The average period of the ringing is $T_r = 440\,\mathrm{ns}$. Thus,

$$\begin{aligned} C_s &= \frac{1}{L}\left(\frac{T_r}{2\pi}\right)^2 \\ &= 137.75\,\mathrm{pF} \end{aligned} \tag{5.14}$$

Snubber Transformer Leakage Inductance (L_a)

When operating with the snubber, (2.33) shows that the ringing frequency of the secondary voltage v_s in the active mode V is $f_{ra} = \frac{1}{\sqrt{L_a C_s}}$. Fig 5.8(b) shows the secondary voltage v_s, where T_{ra} gives the period of oscillations. Thus for $T_{ra} = 121.2\,\text{ns}$, the leakage inductance L_a of the snubber can be calculated as

$$\begin{aligned} L_a &= \frac{1}{C_s}\left(\frac{T_{ra}}{2\pi}\right)^2 \\ &= 2.701\,\mu\text{H} \end{aligned} \tag{5.15}$$

Snubber Bridge Capacitance (C_a)

During the zero state, i.e. mode VIII, the resonant circuit formed between L_a inductance and C_s leads to ringing in the snubber current i_a about zero, as shown in Fig5.8(c). Equation (2.52) shows that the frequency of these oscillations is given by $\omega_3 = \frac{1}{\sqrt{L_a C_a}}$ and is 5.91 MHz. Thus,

$$\begin{aligned} C_a =& \frac{1}{L_a}\left(\frac{1}{\omega_3}\right)^2 \\ & 250.1\,\text{pF} \end{aligned} \tag{5.16}$$

Primary Bridge Capacitance C_p

C_p can be estimated by solving the pole voltage v_p transitions in modes I and VI. Neglecting the magnetising current I_m, (2.9) and (2.44) give the following two equations.

$$t_I = \sqrt{LC_p}\sin^{-1}\left(\frac{V_{dc}\sqrt{C_p}}{nI_o\sqrt{L}}\right)$$

$$t_{VI} = \sqrt{LC_p}\sin^{-1}\left(\frac{V_{dc}\sqrt{C_p}}{nI_o\sqrt{L} + V_{dc}\sqrt{(C_a + C_s)}}\right)$$

Shown in Fig 5.8(b), $t_I = 150\,\text{ns}$ and $t_{VI} = 71\,\text{ns}$ for $V_{dc} = 400\,\text{V}$ and $P_o = 0.5\,\text{kW}$. The C_p is numerically obtained using the two equations and averaged to get

$$C_p = 617.27\,\text{pF}$$

Table 5.3 summarises the parameters estimated using the two methods - FRA and WE. The value of L and range of capacitances C_p, C_s, and C_a in the column of 'Chosen Design Values' are discussed in Section 3.4.

5.3 Verification of the Snubber Operation

The snubber operation is verified using the parameters estimated through the WE method. Therefore, the circuit parameters are $n = 0.25$, $L_a = 2.701\,\mu\text{H}$, $L = 35.267\,\mu\text{H}$, $C_p =$

Table 5.3: Comparison of parameters estimated using FRA and WE to chosen design values.

	Chosen Design Values	Measured (FRA)	Measured (WE)
L	30 µH	35.9 µH	35.267 µH
L_a	2.1 µH	2.94 µH	2.701 µH
C_p	160.7-460.7 pF	-	617.27 pF
C_s	85.7-104.45 pF	-	137.75 pF
C_a	70.25-370.25 pF	-	250.1 pF

617.27 pF, $C_s = 137.75$ pF, and $C_a = 250.1$ pF. As discussed in Chapter 1, the voltage v_s may go up to twice nV_{dc} when the converter is operated without any snubber. Fig 5.9(a) validates the same by operating the PSFB converter without the snubber. The observed overshoot without the snubber is 100 V at $V_{dc} = 400$ V and $n = 0.25$. As discussed in

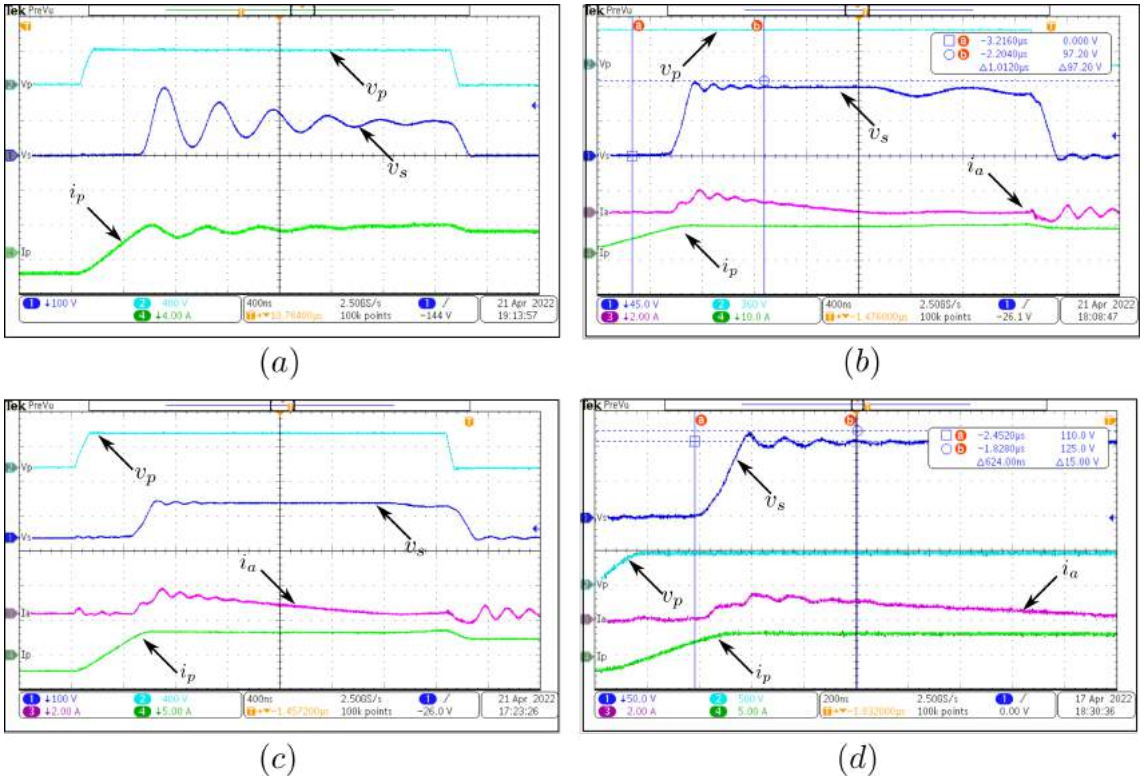


Fig. 5.9: PSFB waveforms (a) without snubber at $V_{dc} = 400$ V (b) with snubber at $V_{dc} = 360$ V (c) with snubber at $V_{dc} = 400$ V (d) with snubber at $V_{dc} = 440$ V

Section 2.2.5; the secondary voltage overshoot is proportional to the leakage inductance of the snubber transformer and the series inductance for soft-switching. It was shown that parasitic capacitances of the secondary and snubber bridge diodes also affect the

overshoots. The magnitude of the overshoot in the ringing, as seen on the transformer secondary terminals, is given by (5.17).

$$n\Delta V_s' = nV_{dc}\sqrt{\frac{L_a}{L}\frac{C_s}{(C_s + C_a)}} \tag{5.17}$$

Fig 5.9(b), Fig 5.9(c), and Fig 5.9(d) show the effectiveness of the snubber in reducing the rectifier bridge voltage overshoots. Table 5.4 Compares the measured and analytical overshoot at $V_{dc} = 360$, 400, and 440 V.

Table 5.4: Secondary Voltage overshoot comparison.

nV_{dc} (V)	Analytical $n\Delta V_s'$ (V)	Experimental $n\Delta V_s'$ (V)
90	14.8	7.2
100	16.5	6.7
110	18.1	15

Fig 5.10 compares the analytically and experimentally obtained snubber current waveform. The snubber current is measured at $V_{dc} = 400$ V, $n = 0.25$, $P_o = 0.5$ kW, and $f_s = 100$ kHz. The analytical solution neglects the damping in snubber circuit oscillations due to various

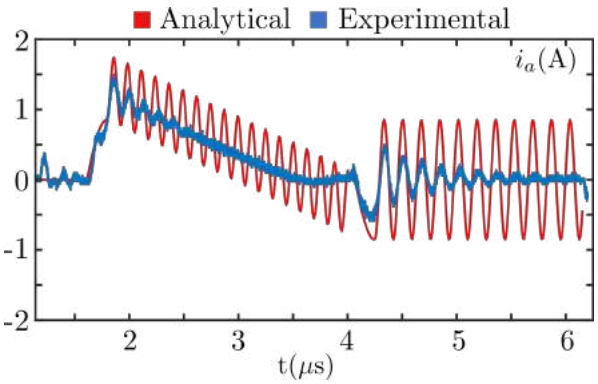


Fig. 5.10: Analytically obtained snubber current i_a fitted over experimentally measured current.

power and snubber circuit losses. Thus, we can observe sustained ringing in the active and passive states. As discussed in Section 2.5.1, the snubber current falls at a rate of

$$\Delta_s = \frac{V_{dc}}{L_m} + \frac{n(nV_{dc} - V_o)}{L_f} \tag{5.18}$$

Where $L_m = 0.74$ mH, is the parallel combination of magnetising inductances L_{mag} of the two transformers estimated in Section 5.2.1. Therefore, for $L_f = 65.52\,\mu$H and $V_o = 48$ V, $\Delta_s = 0.543\,\text{A}\,\mu\text{s}^{-1}$.

5.4 PSFB Design Validation

Table 5.5: PSFB measured parameters

Parameter	L (µH)	L_a (µH)	C_p (pF)	C_s (pF)	C_a (pF)	f_s (kHz)	n
Value	35.267	2.701	617.27	137.75	250.1	100	0.25

Table 5.5 contains the measured parameters using the WE method. The PSFB operation is verified using the parameters in the table. The designed PSFB is desired to produce 48 V output at 0.5-1.5 kW, given that the input DC bus voltage varies between 360-440 V.

As explored in Chapter 3, the following two design objectives must be satisfied to validate the converter design procedure.

- **Objective I:** Converter must produce the required gain, with the analytically derived duty using (3.12).
- **Objective II:** All inverter switches should achieve ZVS turn ON for the desired operating conditions.

5.4.1 Objective I: The Converter Gain Verification

In Section 3.2, we analysed that the two extreme operating conditions - Condition I ($V_{dc} = 360$ V, $P_o = 1.5$ kW) and Condition II ($V_{dc} = 440$ V, $P_o = 0.5$ kW) accomplish the desired output voltage with maximum and minimum duty ratio, respectively. The experiment

Table 5.6: Analytical v/s Experimental mode interval comparison for Condition I ($V_{dc} = 360$ V, $P_o = 1.5$ kW) and Condition II ($V_{dc} = 440$ V, $P_o = 0.5$ kW).

Mode Interval	$V_{dc} = 360$ V, $P_o = 1.5$ kW		$V_{dc} = 440$ V, $P_o = 0.5$ kW	
	Analytical	Experimental	Analytical	Experimental
$t_I = t_1 - t_o$	29.9 ns	28 ns	160 ns	184 ns
$t_{II} = t_2 - t_1$	718.6 ns	645 ns	78 ns	37 ns
$t_{III} = t_3 - t_2$	733.6 ns	744 ns	167 ns	173 ns
$t_{IV} = t_4 - t_3$	183.71 ns	173 ns	183.71 ns	170 ns
$t_V = t_5 - t_4$	2490.4 ns	2601 ns	2005.5 ns	2034 ns
$t_{VI} = t_6 - t_5$	25.72 ns	24 ns	80.64 ns	72 ns
$t_{VII} = t_7 - t_6$	183.71 ns	175 ns	183.71 ns	138 ns
$t_{VIII} = t_8 - t_7$	634.36 ns	610 ns	2141.44 ns	2192 ns
d	0.8315	0.8382	0.5188	0.5196

adjusts duty cycles in the open loop to achieve 48 V output. Experimentally measured time intervals of the different modes are given in Table 5.6. Following the analysis in

Chapter 2, these time intervals are also computed using the experimentally measured parameters. The ratio of the period of the switching instants of the two legs to half the switching cycle specifies the duty d. Thus,

$$d = \frac{t_I + t_{II} + t_{III} + t_{IV} + t_V}{T_s/2} \tag{5.19}$$

It is noteworthy that the open loop adjusted duty cycle is close to its analytically predicted value confirming the output voltage expression (2.55). Also, the extreme duty cycles that appear for the two extreme operating conditions are within the specified limits (d_{min}, d_{max}) from Chapter 3, confirming proper design choices of L and n.

Fig 5.11 shows the experimentally measured state variable waveforms at two extreme operating conditions. All of the modes are clearly visible. Fig 5.12 compares the analytically driven and experimentally measured waveforms. The analytical waveforms neglect the damping of high-frequency oscillations in v_s during the active state. A close match between the quantities in Table 5.6 and a close resemblance of the waveforms in Fig 5.12 confirms the analysis of Chapter 2.

Fig 5.12(a) shows a low-frequency ringing in v_s towards the end of the active state. As discussed in Section 2.5, this starts after the snubber current i_a falls to zero before t_5. However, contrary to the discussion in the section, this i_a fall seems dependent on the load current. The DC bias characteristics in the datasheet of the toroidal core (Magnetics 0077617A7) reveal a 30% decrement in the permeability at the full load current, reducing the filter inductance L_f. The reduction in L_f leads to an increase in output current ripple, and as discussed in Section 2.5, it increases the i_a fall rate. Consequently, changing the decay rate of the snubber current with a change in loading conditions.

Although the experimental results for the two mentioned operating conditions are necessary and sufficient to verify the converter design, to substantiate the Table 5.7 compares the experimental and analytical duty cycles required for the operating conditions between the two extreme cases of Condition I and Condition II. The required duty cycles for these operating conditions also lie between the duty ratios of the two extreme operating conditions.

Additionally, the following things can be inferred using the data in Table 5.6 and Table 5.7.

- As the load increases, the lag and lead leg switching time intervals become approximately equal. It reduces the significance of the third term in (2.55), as discussed in Section 2.3.
- The analytical time intervals of v_s rise and fall are same. However, the mismatch in the experimental intervals is mainly due to the change in the initial conditions of v_s during mode VII. This change of initial conditions occurs due to low-frequency oscillations in v_s after the i_a goes to zero.

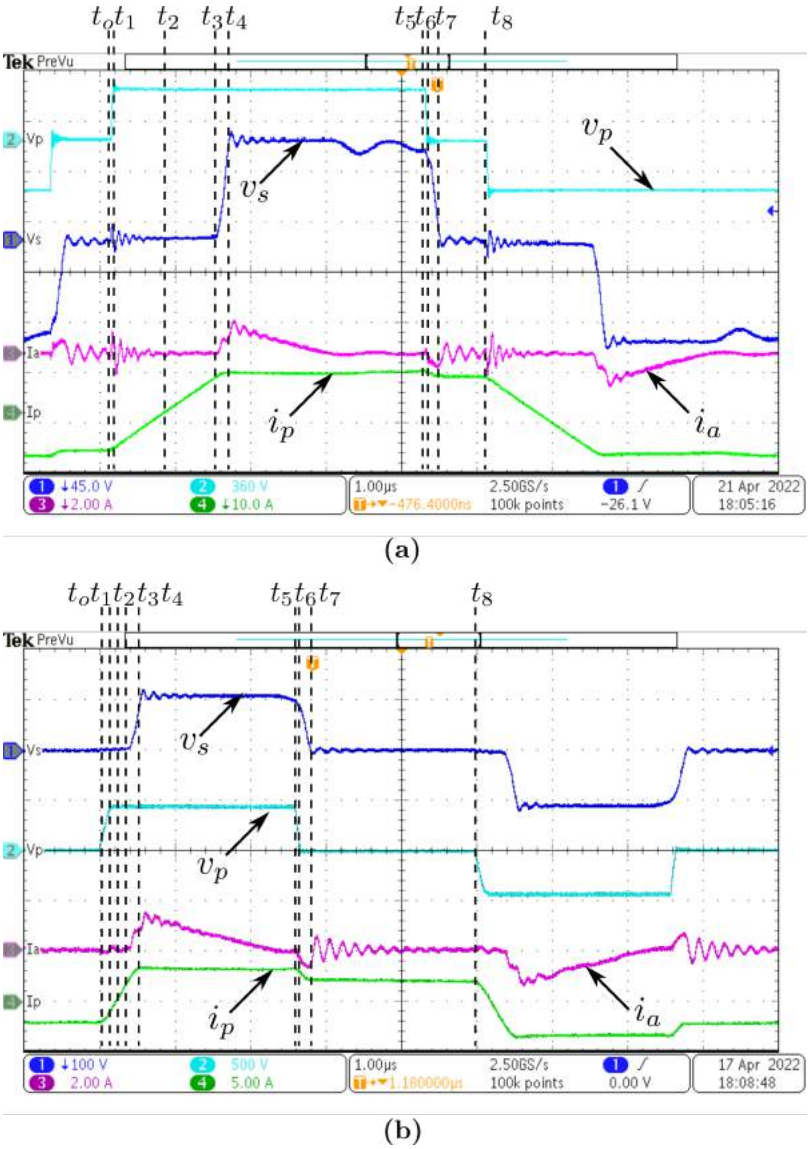


Fig. 5.11: Converter state variable waveforms. (a) $V_{dc} = 360\,\text{V}$, $P_o = 1.5\,\text{kW}$ (b) $V_{dc} = 440\,\text{V}$, $P_o = 0.5\,\text{kW}$

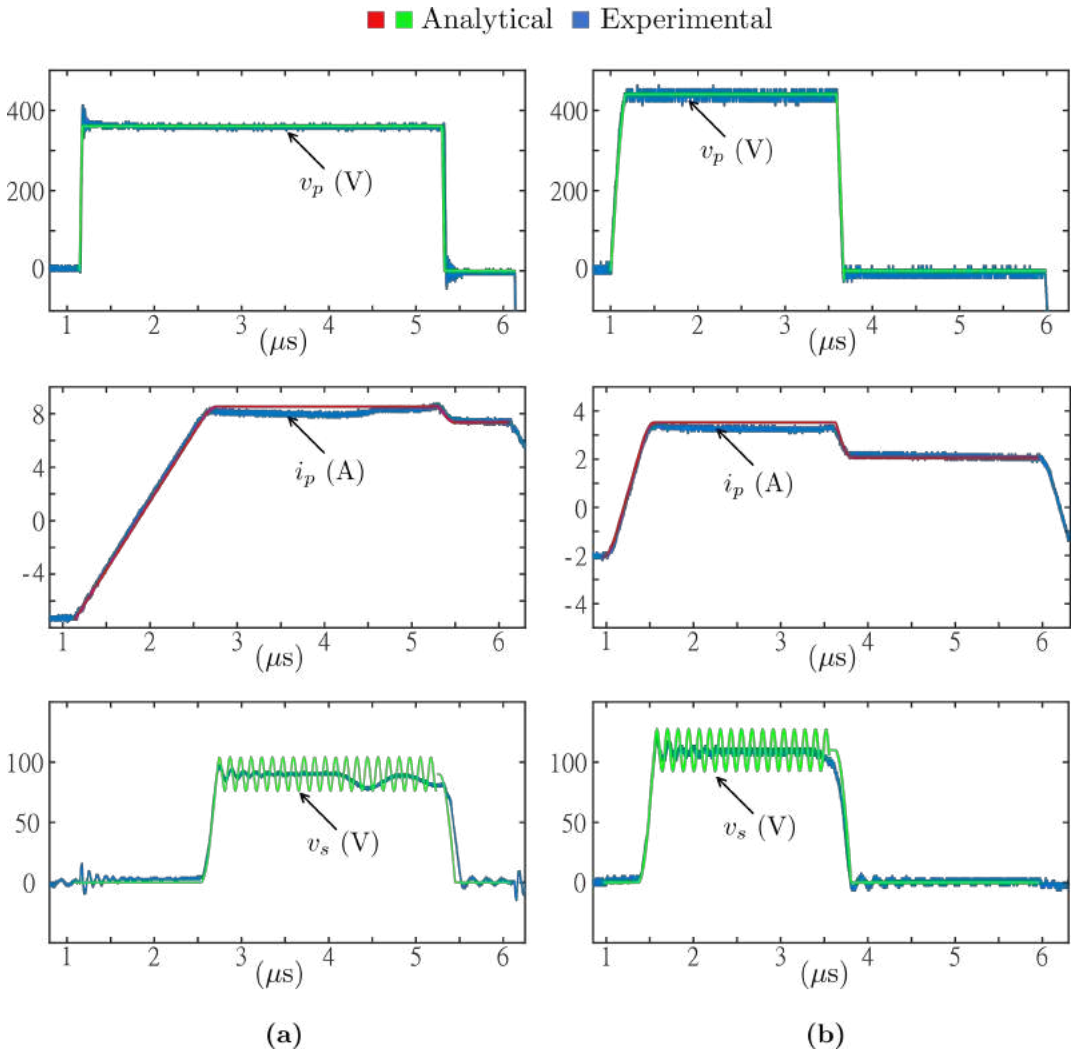


Fig. 5.12: Comparison of analytical and experimental converter waveforms. (a) $V_{dc} = 360\,\text{V}$, $P_o = 1.5\,\text{kW}$ (b) $V_{dc} = 440\,\text{V}$, $P_o = 0.5\,\text{kW}$

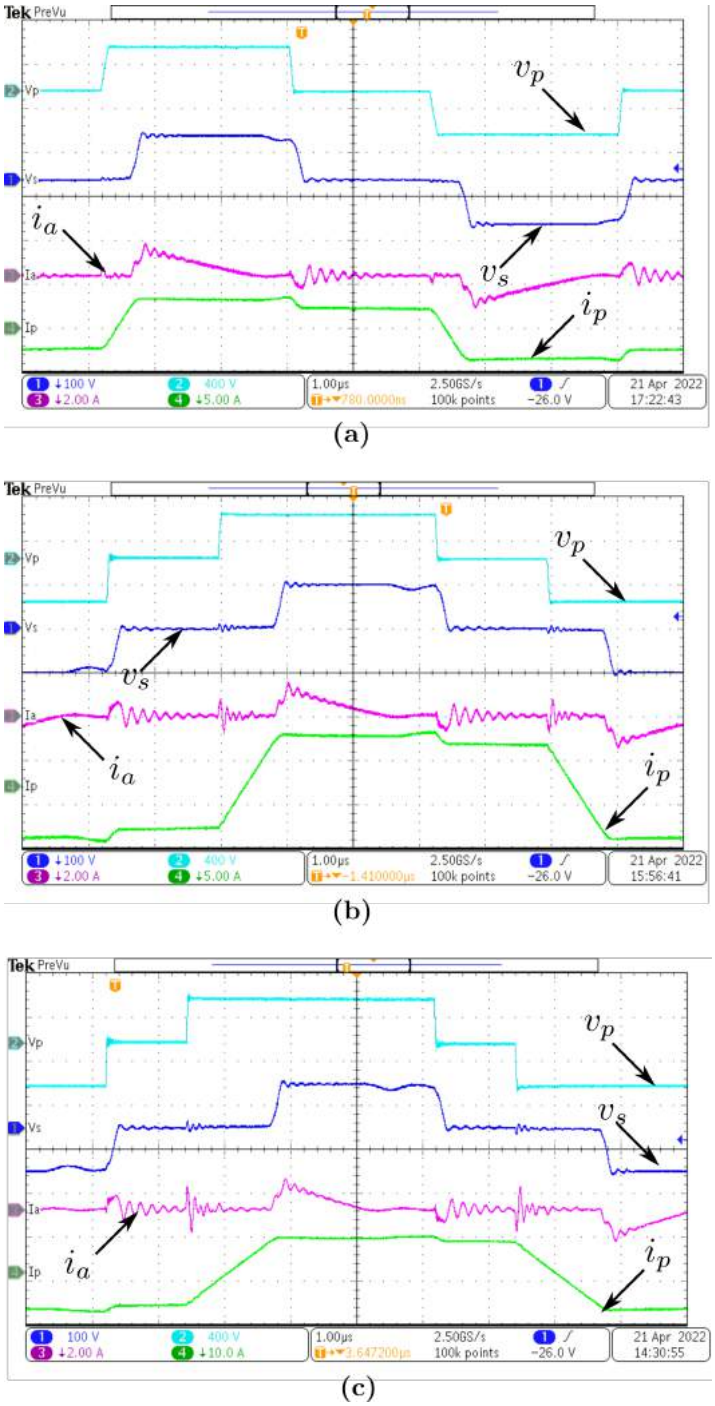


Fig. 5.13: Converter variables at a DC bus voltage of 400 V. (a) $P_o = 0.5\,\text{kW}$ (b) $P_o = 1\,\text{kW}$ (c) $P_o = 1.5\,\text{kW}$

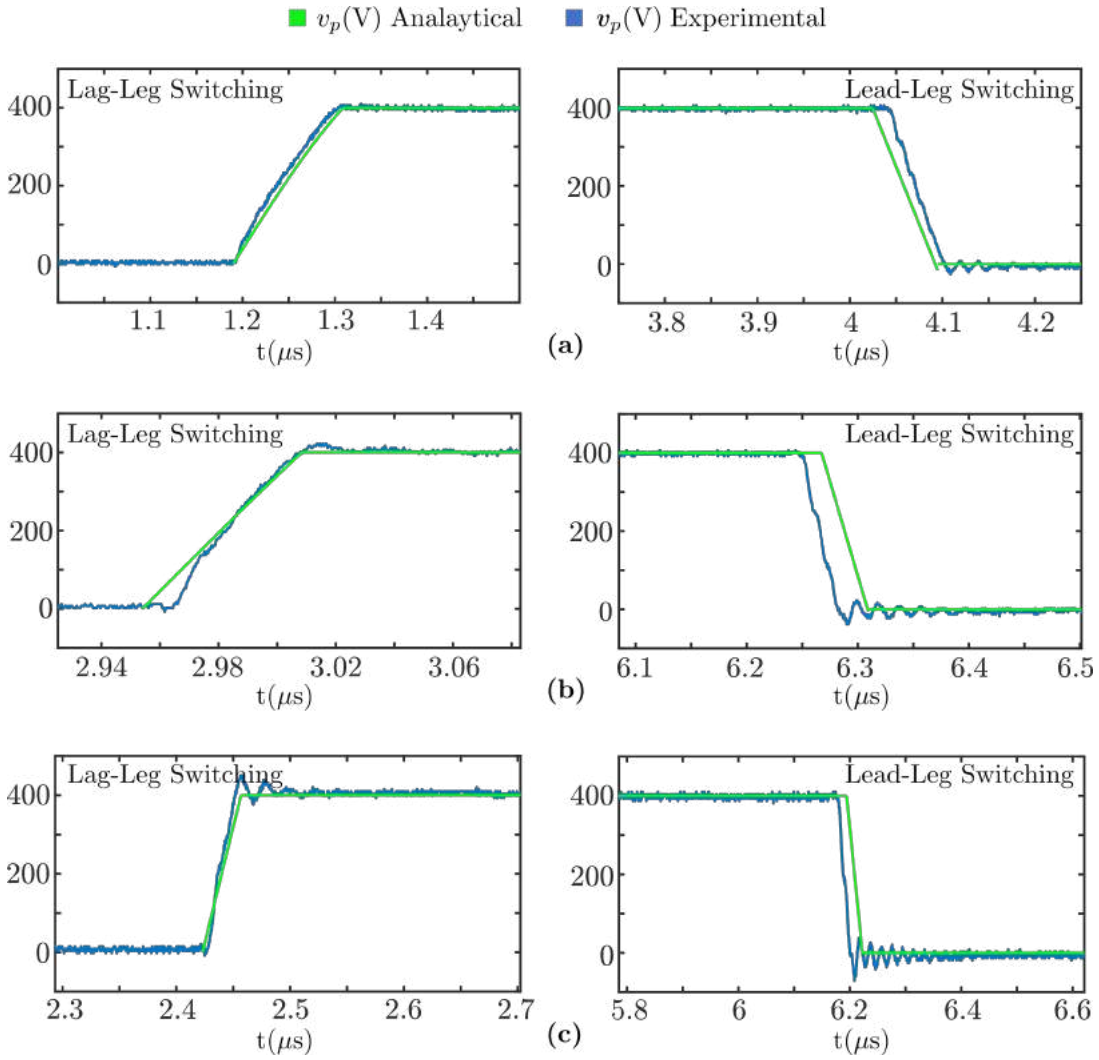


Fig. 5.14: Pole Voltage v_p rise and fall during lag and lead leg switching, respectively. (a) $V_{dc} = 400\,\text{V}$, $P_o = 0.5\,\text{kW}$ (b) $V_{dc} = 400\,\text{V}$, $P_o = 1\,\text{kW}$ (c) $V_{dc} = 400\,\text{V}$, $P_o = 1.5\,\text{kW}$

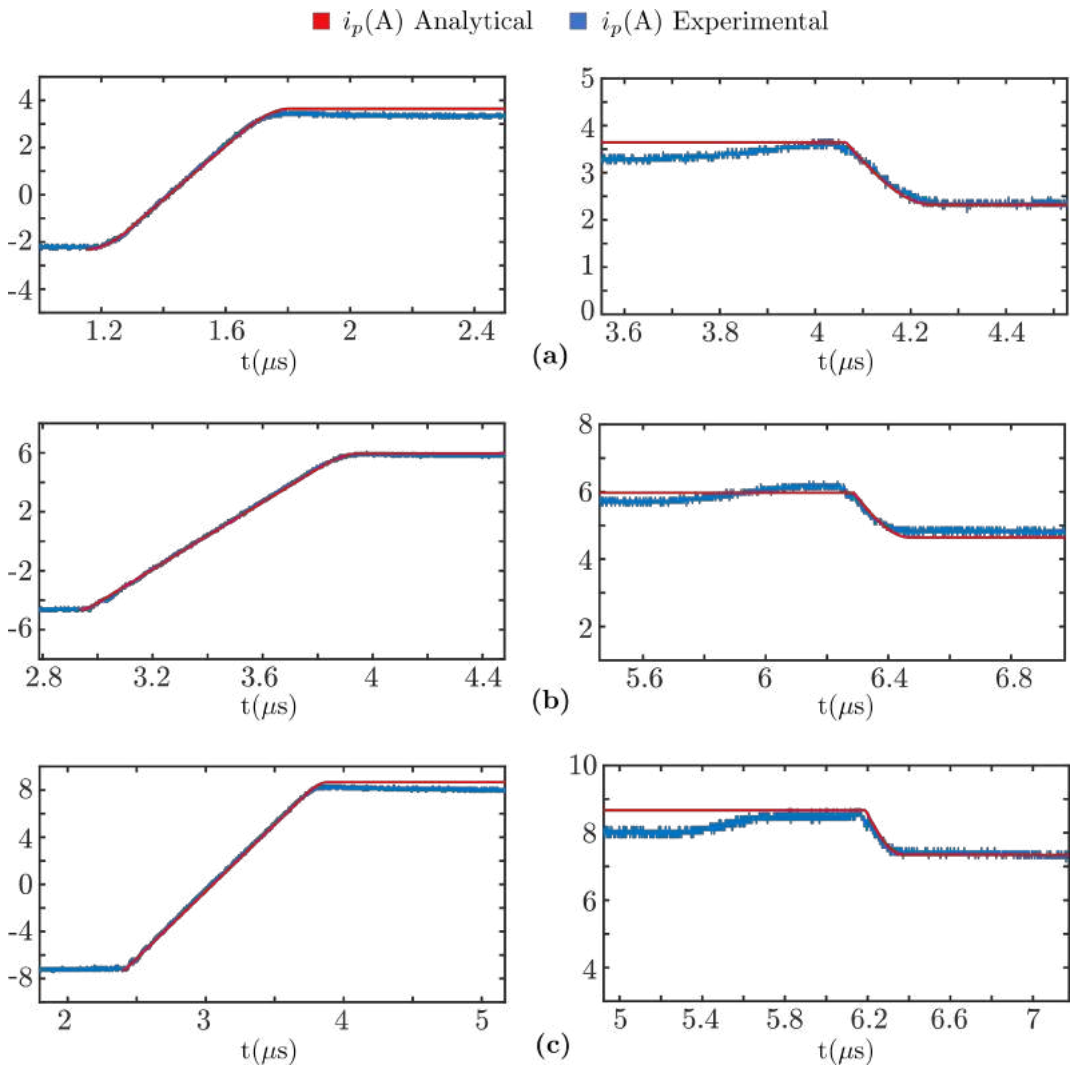


Fig. 5.15: Primary Current i_p transitions after lag[left plot] and lead[right plot] switching. (a) $V_{dc} = 400\,\text{V}$, $P_o = 0.5\,\text{kW}$ (b) $V_{dc} = 400\,\text{V}$, $P_o = 1\,\text{kW}$ (c) $V_{dc} = 400\,\text{V}$, $P_o = 1.5\,\text{kW}$

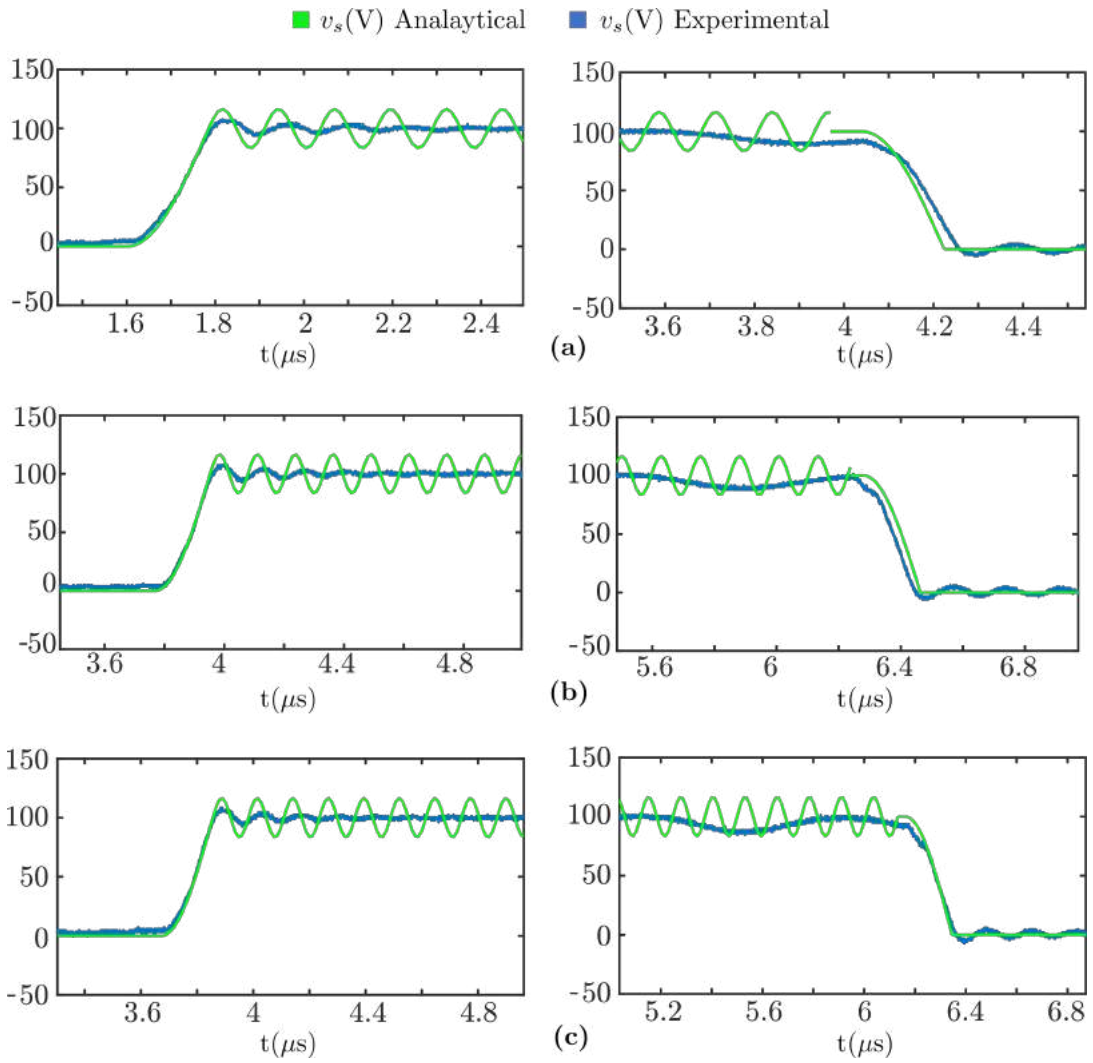


Fig. 5.16: Secondary voltage v_s rise and fall transitions with active state voltage overshoots. (a) $V_{dc} = 400\,\text{V}$, $P_o = 0.5\,\text{kW}$ (b) $V_{dc} = 400\,\text{V}$, $P_o = 1\,\text{kW}$ (c) $V_{dc} = 400\,\text{V}$, $P_o = 1.5\,\text{kW}$

Table 5.7: Analytical v/s experimental mode interval comparison for converter operating at $V_{dc} = 400\,\text{V}$ and $P_o \in [0.5\,\text{kW} - 1.5\,\text{kW}]$.

Mode Interval	400 V, 0.5 kW		400 V, 1 kW		400 V, 1.5 kW	
	Anly.	Exp.	Anly.	Exp.	Anly.	Exp.
$t_I = t_1 - t_o$	125.36 ns	120 ns	52.7 ns	54 ns	33.2 ns	30 ns
$t_{II} = t_2 - t_1$	129.71 ns	104 ns	395 ns	352 ns	644.55 ns	581 ns
$t_{III} = t_3 - t_2$	196.45 ns	211 ns	421.7 ns	421 ns	661.22 ns	678 ns
$t_{IV} = t_4 - t_3$	183.71 ns	165 ns	183.71 ns	182 ns	183.71 ns	150 ns
$t_V = t_5 - t_4$	2222 ns	2249 ns	2260.3 ns	2283 ns	2248.5 ns	2315 ns
$t_{VI} = t_6 - t_5$	72.322 ns	61 ns	40.93 ns	37 ns	28.14 ns	24 ns
$t_{VII} = t_7 - t_6$	183.71 ns	156 ns	183.71 ns	162 ns	183.71 ns	161 ns
$t_{VIII} = t_8 - t_7$	1886.7 ns	1934 ns	1462 ns	1509 ns	857 ns	880 ns
d	0.5715	0.5698	0.663	0.6584	0.7542	0.7510

Fig 5.14 shows pole voltage v_p during Passive to Active and Active to Passive transitions for a nominal DC bus voltage of 400V and output power of 0.5, 1, and 1.5 kW. Similarly, Fig 5.15 and Fig 5.16 show the primary current i_p and the secondary voltage v_s dynamics for the three power levels at $V_{dc} = 400\,\text{V}$.

5.4.2 Objective II: Inverter Switches ZVS Turn-ON

As discussed in Chapter 3, the results of the converter operation at maximum input voltage and minimum output power are sufficient to validate the ZVS of inverter switches. Fig 5.17(a) and Fig 5.17(b) show v_p and i_p at $V_{dc} = 440\,\text{V}$ and $P_o = 0.5\,\text{kW}$. During the period when $v_p = 0$, switches Q_2 and Q_4 are in conduction, operating in the passive state. The lag-leg's bottom switch Q_2 is turned OFF and voltage v_p rises to V_{dc} due to simultaneous charging and discharging of C_2 and C_1, respectively. The smooth rise of voltage v_p and reaching V_{dc} before i_p reaches zero validates the sufficiency of available magnetic energy for passive to active mode transition. Scope data for v_p and i_p is plotted in Fig 5.17(c). Fig 5.17(a) and Fig 5.17(b) show the experimentally calculated limits on the

Table 5.8: Experimental and Analytical dead time comparison.

	$t_{d,min}$ (ns)	$t_{d,max}$ (ns)
Experimental	160	226
Analytical	143.9	243.9

dead time. The minimum limit $t_{d,min}$ is measured as the time taken from the turn-OFF of Q_2 to voltage v_p reaching V_{dc} while $t_{d,max}$ is the time interval from the switching instant to the instant, current i_p reduces to zero. The analytical limits on the dead time can be derived using (3.14). Table 5.8 compares the experimental and analytical dead time limits.

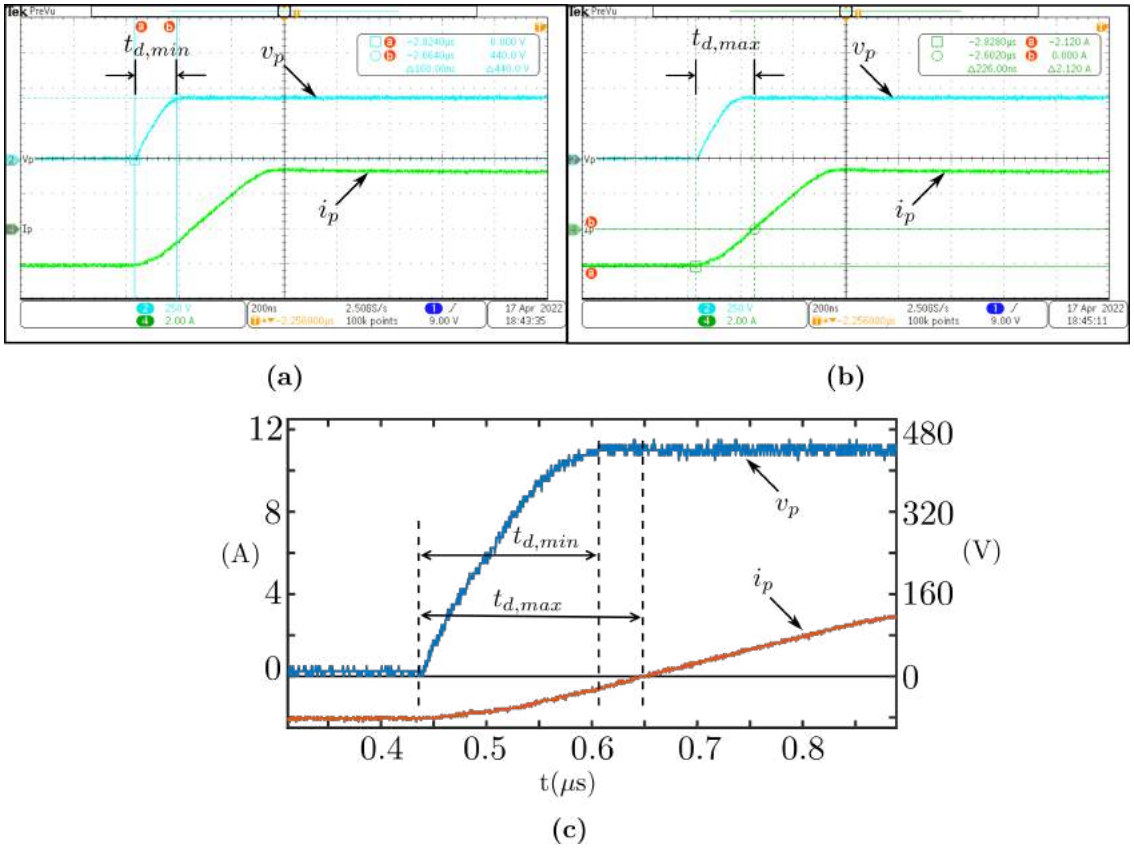
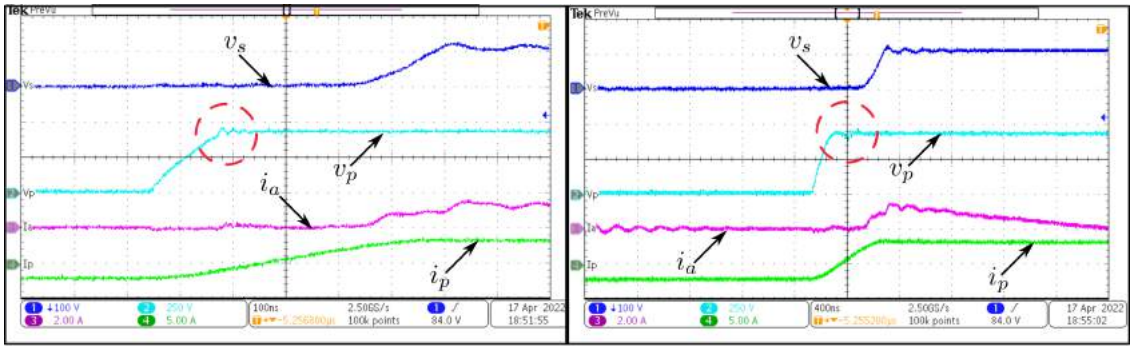
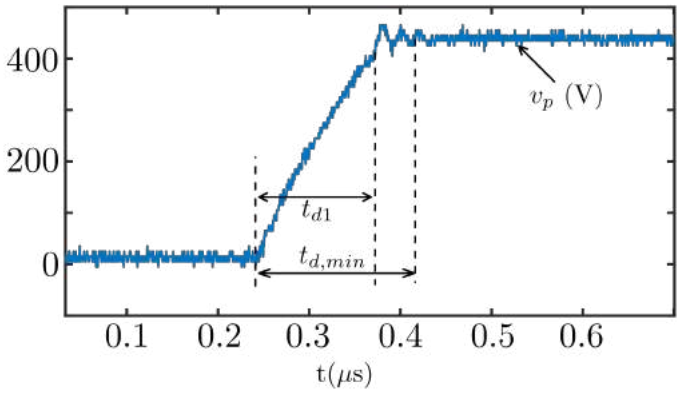


Fig. 5.17: Pole voltage v_p and primary current i_p waveforms at $V_{dc} = 440\,\text{V}$ and $P_o = 0.5\,\text{kW}$. (a) and (b) Measured voltage v_p shows a smooth rise to V_{dc}. The minimum and maximum dead times are marked as $t_{d,min}$ and $t_{d,max}$, respectively. (c) MATLAB plot using experimental data shows the lag-leg switching transition.

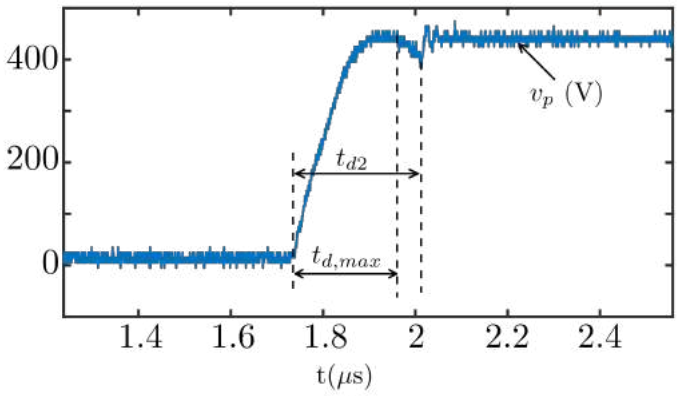
Fig 5.18(a) and Fig 5.18(b) show the lag-leg devices losing zero voltage switching as dead time selected crosses the $t_{d,min}$ and $t_{d,max}$ limits, respectively. Fig 5.18(c) shows the scope data plot of voltage v_p for the dead time $t_{d1} = 142$ ns being less than $t_{d,min}$. A dead time less than $t_{d,min}$ does not allow the complete charging and discharging of C_2 and C_1, respectively. The current starts flowing through the channel of the device Q_1 without its drain to source voltage V_{ds} reducing to zero. Thus, resulting in partial soft-switching.
Fig 5.18(d) shows the inverter leg devices switching with a dead time $t_{d2} = 267$ ns being more than $t_{d,max}$. With the switch Q_1 still ON after i_p reaches zero, the current reverses its direction, resulting in charging of C_1 and C_2 again. Turning ON switch Q_1 at this moment pushes the current through its channel when V_{ds} is non-zero, losing soft-switching in the devices.



(a) (b)



(c)



(d)

Fig. 5.18: Partial ZVS turn ON (a), (c) chosen dead time $t_{d1} < t_{d,min}$ and (b), (d) $t_{d2} > t_{d,max}$.

5.5 Converter Efficiency and Loss Budgeting

The converter efficiency is measured at nominal input and output voltage of 400 V and 48 V, respectively, at different power levels with Tektronix power analyser PA3000. Fig 5.19 shows the efficiency plot of the developed PSFB converter. It achieves a peak efficiency of around 93% at 750 W. At a rated load of 1.5 kW the efficiency is around 92%.

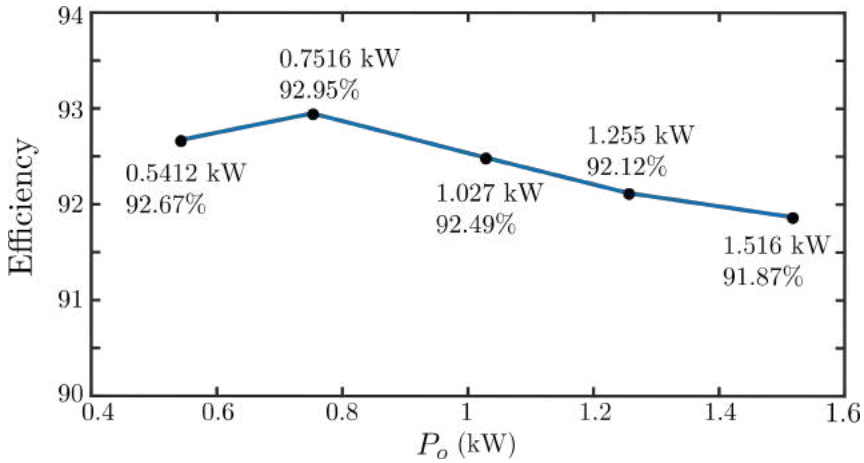


Fig. 5.19: Efficiency v/s Output-Power

The following section covers the loss distribution among the different elements of the converter. The general division of the power loss is estimated for the following components of the PSFB.

5.5.1 Inverter bridge Losses

Conduction losses of the primary devices are estimated, assuming negligible switching losses in the inverter bridge. The ON-state resistance R_{ds} can be extracted from the R_{ds} v/s drain current curves in the MOSFET datasheet. Thus, the conduction loss $P_{inverter}$ of the inverter bridge is expressed as in (5.20).

$$P_{inverter} = 4(\frac{I_{p,rms}}{\sqrt{2}})^2 R_{ds} \tag{5.20}$$

Where $I_{p,rms}$ is the RMS value of the measured primary current and R_{ds} at different primary currents, shown in Table 5.9.

5.5.2 Series Inductor Losses

FRA on the external series inductor (B82559A0303A024) is conducted to obtain the coil resistance at different frequencies. Discrete Fourier Transform (DFT) of the measured

Table 5.9: Primary bridge conduction losses.

P_o	0.541 kW	0.752 kW	1.027 kW	1.255 kW	1.516 kW
$I_{p,rms}$ (A)	2.82	3.74	5.1	6.05	7.16
R_{ds} (Ω)	0.15	0.152	0.154	0.156	0.158
$P_{inverter}$ (W)	2.385	4.26	7.946	11.43	16.21

primary current gives its corresponding amplitude spectrum. Equation (5.21) expresses the conduction loss contribution of the inductor $P_{inductor}$.

$$P_{inductor} = \sum_{i=1}^{\infty} \left(\frac{I_{p,i}}{\sqrt{2}}\right)^2 R_{s,i} \tag{5.21}$$

The fundamental frequency being 100 kHz, $I_{p,i}$ is the primary current's ith harmonic peak amplitude, and $R_{s,i}$ is the corresponding coil resistance. Table 5.10 shows the $I_{p,i}$ and $R_{s,i}$ at different power levels. The last row of the table displays the conduction loss of the externally added series inductor.

Table 5.10: Series inductor conduction losses for primary currents at different power levels.

		$I_{p,i}$ (A)				
Harmonics	$R_{s,i}$ (Ω)	P_o 0.541 kW	P_o 0.752kW	P_o 1.027 kW	P_o 1.255 kW	P_o 1.516 kW
1	0.555	3.726	5	6.859	8.244	9.827
3	1.07	1.075	1.351	1.771	2	2.229
5	1.58	0.7393	0.9453	1.081	1.064	0.9032
7	2.03	0.3432	0.3522	0.3361	0.2632	0.1591
9	2.89	0.3568	0.3751	0.2243	0.1038	0.2515
11	4.12	0.1208	0.08947	0.09528	0.1128	0.1341
13	6.38	0.1818	0.1189	0.1156	0.1938	0.1293
15	10.5	0.02006	0.06153	0.06997	0.0459	0.04575
17	13.8	0.08128	0.04983	0.1202	0.04821	0.09456
$P_{inductor}$ (W)		5.39	9.05	16.0	22.2	30.4

The inductor datasheet does not provide any information regarding the core material and the core dimensions. Therefore, core loss calculations could not be carried out.

5.5.3 Main Transformer Losses

Copper loss:
A similar approach, as discussed in Section 5.5.2 is followed to estimate the main transformer winding losses. Table 5.11 summarises the $I_{p,i}$ and corresponding R_i at different power levels where R_i is the winding resistance referred to primary for the ith harmonic current. These winding resistances are obtained through FRA of the driving point

impedance on the HV side shorting the LV terminals. Equation (5.22) expresses the conduction loss contribution of the main transformer $P_{cu,main}$.

$$P_{cu,main} = \sum_{i=1}^{\infty} \left(\frac{I_{p,i}}{\sqrt{2}}\right)^2 R_i \tag{5.22}$$

Table 5.11: Main Transformer conduction losses for primary currents at different power levels.

		$I_{p,i}$ (A)				
Harm-onics	R_i (Ω)	P_o 0.541 kW	P_o 0.752 kW	P_o 1.027 kW	P_o 1.255 kW	P_o 1.516 kW
1	0.0663	3.726	5	6.859	8.244	9.827
3	0.153	1.075	1.351	1.771	2	2.229
5	0.309	0.7393	0.9453	1.081	1.064	0.9032
7	0.316	0.3432	0.3522	0.3361	0.2632	0.1591
9	0.474	0.3568	0.3751	0.2243	0.1038	0.2515
11	0.631	0.1208	0.08947	0.09528	0.1128	0.1341
13	0.845	0.1818	0.1189	0.1156	0.1938	0.1293
15	1.14	0.02006	0.06153	0.06997	0.0459	0.04575
17	1.33	0.08128	0.04983	0.1202	0.04821	0.09456
$P_{cu,main}$ (W)		0.705	1.17	2.03	2.77	3.75

Core Loss:
The improved General Steinmetz Equation (5.23) gives the power loss density (P_v) for non-sinusoidal flux density waveforms.

$$P_v = K_i |\Delta B|^{\beta-\alpha} \frac{1}{T_s} \int_0^{T_s} \left|\frac{dB(t)}{dt}\right|^{\alpha} dt \tag{5.23}$$

Where $\Delta B = 2B_{max}$ is the peak to peak flux density and T_s is the switching period. K_i is given by

$$K_i = \frac{K_c}{2^{\beta-1}\pi^{\alpha-1}\left(1.1044 + \frac{6.8244}{\alpha+1.354}\right)} \tag{5.24}$$

The core material used for the main transformer is N87. The above material coefficients $\alpha = 1.252$, $\beta = 2.322$, and $K_c = 82.8436$ can be determined from the core's datasheet, as shown in [36]. B_m can be calculated using (5.25) for $V_{dc} = 400\,\text{V}$, $D_{eff} = V_o/(nV_{dc})$, $N_p = 12$, $A_c = 529\,\text{mm}^2$, $V_o = 48\,\text{V}$, and $f_s = 100\,\text{kHz}$. D_{eff} is the effective duty ratio to attain desired output voltage after subtracting all the losses from the applied duty. Using (5.24), $K_i = 16$ while P_v can be calculated using (5.26) as follows.

$$\begin{aligned} B_m &= \frac{V_{dc} D_{eff}}{4 f_s N_p A_c} \\ &= 0.076\,\text{T} \end{aligned} \tag{5.25}$$

$$P_v = K_i|\Delta B|^{\beta-\alpha} f_s \left\{ |2\Delta B|^{\alpha} \left(\frac{D_{eff}}{f_s} \right)^{1-\alpha} \right\} \\ = 76.84\,\mathrm{kW/m^3} \tag{5.26}$$

The volume of the main transformer's core is $78.65\,\mathrm{cm}^3$, which gives the core loss to be $P_{core,main} = 6.043\,\mathrm{W}$.

The total loss contribution P_{T_m} of the main transformer is summed up in Table 5.12.

Table 5.12: Total power loss in the main transformer.

P_o	0.541 kW	0.752 kW	1.027 kW	1.255 kW	1.516 kW
P_{T_m} (W)	6.748	7.213	8.073	8.813	9.793

5.5.4 Secondary Diode Bridge Losses

Table 5.13: Conduction losses in the rectifier Bridge.

P_o	0.541 kW	0.752 kW	1.027 kW	1.255 kW	1.516 kW
I_o (A)	11.39	15.558	21.579	26.198	31.872
V_f (V)	0.59	0.61	0.64	0.66	0.68
R_d (mΩ)	6.25	6.25	6.25	6.25	6.25
$P_{rectifier}$ (W)	15.06	22.01	33.44	43.16	56.04

Devices used in the secondary bridge of the converter are Si Schottky barrier diodes. Assuming minimal switching losses in SBDs, (5.27) expresses the conduction loss contribution of the rectifier bridge $P_{rectifier}$.

$$P_{rectifier} = 4 \left[\frac{I_o}{2} V_f + \left(\frac{I_o}{\sqrt{2}} \right)^2 R_d \right] \tag{5.27}$$

5.5.5 Output Choke Losses

Copper Loss:
The ripple in the output current is small, and thus, the high-frequency copper loss is neglected. The measured DC resistance of the inductor is $R_{dc} = 4\,\mathrm{m\Omega}$. Equation (5.33) calculates the copper loss $P_{f,cu}$ in the output choke, while Table 5.14 shows the output current RMS I_o values and the conduction losses of the inductor coil.

$$P_{f,cu} = I_o^2 R_{dc} \tag{5.28}$$

Table 5.14: Filter choke conduction losses.

P_o	0.541 kW	0.752 kW	1.027 kW	1.255 kW	1.516 kW
I_o (A)	11.39	15.558	21.579	26.198	31.872
R_{dc} (mΩ)	4	4	4	4	4
$P_{f,cu}$ (W)	0.52	0.97	1.86	2.75	4.06

Core Loss:
The peak to peak magnetic flux density ΔB in the output filter core is given by

$$\begin{aligned}\Delta B &= \frac{(nV_{dc} - V_o)D_{eff}}{2f_s N A_c} \\ &= 0.018\,24\,\mathrm{T}\end{aligned} \tag{5.29}$$

Where $V_o = 48\,\mathrm{V}$ is the average output voltage, $N = 19$ is the number of turns, and $A_c = 360\,\mathrm{mm}^2$ expresses the core's cross-sectional area. $D_{eff} = V_o/(nV_{dc})$ and $f_s = 100\,\mathrm{kHz}$ represent the effective duty and switching frequency, respectively. The GSE (5.30) gives the formula for the power loss density P_{fe}.

$$\begin{aligned}P_{fe} &= K_c(2f_s)^{\alpha}(\Delta B/2)^{\beta} \\ &= 13.701\,\mathrm{mW/cm}^3\end{aligned} \tag{5.30}$$

Material constants like $K_c = 44.3$, $\beta = 1.988$, and $\alpha = 1.541$ are found in the datasheet of the toroidal core (0077617A7) used. The volume of the core is $V_e = 51\,800\,\mathrm{mm}^3$. Therefore, the core loss $P_{f,core}$ is 0.71 W.
The total loss contribution P_{filter} of the filter inductor is summed up in Table 5.15.

Table 5.15: Total loss contribution of the output choke.

P_o	0.54 1kW	0.752 kW	1.027 kW	1.255 kW	1.516 kW
P_{filter} (W)	1.23	1.68	2.57	3.45	4.77

5.5.6 Snubber Losses

The snubber circuit consists of a diode bridge and a transformer. The following section discusses their individual loss distribution.

Snubber Transformer Copper Loss:
FFT gives the peak-amplitude spectrum of the measured snubber current. Obeying a similar approach as in Section 5.5.3 to estimate the conduction losses in the snubber transformer, Table 5.16 shows the ith harmonics of the snubber current $I_{a,i}$ along with

the winding resistance $R_{a,i}$ referred to the HV side and total conduction loss $P_{cu,snb}$ at different power levels.

$$P_{cu,snb} = \sum_{i=1}^{\infty} \left(\frac{I_{a,i}}{\sqrt{2}}\right)^2 R_{a,i} \tag{5.31}$$

Table 5.16: Snubber Transformer conduction losses for snubber currents at different power levels.

		$I_{a,i}$ (A)				
Freq. (kHz)	$R_{a,i}$ (Ω)	P_o 0.541 kW	P_o 0.752 kW	P_o 1.027 kW	P_o 1.255 kW	P_o 1.516 kW
1	0.14	0.4276	0.4007	0.3859	0.3632	0.3258
3	0.242	0.3515	0.3361	0.3321	0.3204	0.2968
5	0.316	0.1443	0.1508	0.1608	0.172	0.1752
7	0.424	0.128	0.1275	0.1365	0.1442	0.1503
9	0.605	0.06968	0.06751	0.06659	0.05627	0.04041
11	0.788	0.09481	0.1043	0.1058	0.1091	0.1095
$P_{cu,snb}$ (mW)		53.7	51.7	55.1	54.6	48.5

Snubber Transformer Core Loss:
The ferrite material used for the snubber core is the same as the main transformer, i.e. N87. For $N_p = 16$, $A_c = 368\,\text{mm}^2$, and other parameters same as the main transformer, using (5.25), $B_m = 0.082$ T. Using (5.26) the calculated power loss density is $P_v = 91.66$ kW/m^3. Therefore for a core of the volume $V_e = 51200$ mm^3, core loss is

$$P_{core,snb} = 4.7\,\text{W} \tag{5.32}$$

Snubber Bridge Conduction Loss:

Table 5.17: Snubber diode bridge conduction losses.

P_o	0.541 kW	0.752 kW	1.027 kW	1.255 kW	1.516 kW
$I_{a,rms}$ (A)	0.444	0.431	0.432	0.424	0.401
$\lvert I_a\rvert_{avg}$ (A)	0.28	0.29	0.28	0.27	0.2527744
V_f (V)	1	1	1	1	1
R_d (Ω)	0.05	0.05	0.05	0.05	0.05
$P_{snb,bridge}$ (W)	0.582	0.575	0.576	0.562	0.522

The snubber bridge uses SiC SBDs (E3D20065D). Conduction loss of the diode bridge is expressed by (5.33).

$$P_{snb,bridge} = 4\left[\frac{|I_a|_{avg}}{2} V_f + \left(\frac{I_{a,rms}}{\sqrt{2}}\right)^2 R_d\right] \tag{5.33}$$

Where $|I_a|_{avg}$ and $I_{a,rms}$ are the average and RMS values of the snubber current over a switching period, respectively. The forward voltage drop V_f and resistance R_d of the SBD are determined from the forward characteristics given in the snubber diode datasheet. Table 5.17 shows the snubber currents with corresponding V_f , R_d, and conduction losses at different output power. The total loss contribution of the snubber $P_{snubber}$ for different output powers is given in Table 5.18.

Table 5.18: Total loss contribution of the snubber circuit.

P_o	0.541 kW	0.752 kW	1.027 kW	1.255 kW	1.516 kW
$P_{snubber}$ (W)	5.34	5.33	5.33	5.32	5.27

5.5.7 Total Losses Distribution

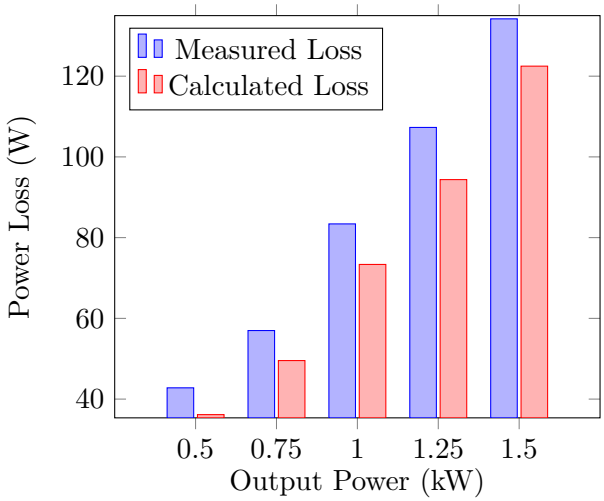


Fig. 5.20: Measured and calculated loss comparison

Fig 5.20 reveals the difference between the measured and calculated losses (without series choke core loss). Fig 5.21 shows the overall loss distribution between different converter components. It is pretty evident from the pie charts that the secondary diode bridge rectifier and the series inductor contribute a significant portion to the total converter loss. Losses in these elements can go up to around 40% and 22%, respectively, at rated load. It is noteworthy that this does not include external inductor core losses. One possible solution to increase the efficiency of the PSFB could be synchronous rectification for the secondary diode bridge. Equation (5.32) and Table 5.18 show that 90% of the snubber loss can be ascribed to the snubber transformer's core loss. Thus, further snubber design improvements are required to make the snubber more efficient. Nonetheless, the total loss in the snubber is constant as the conduction losses in the snubber transformer and the

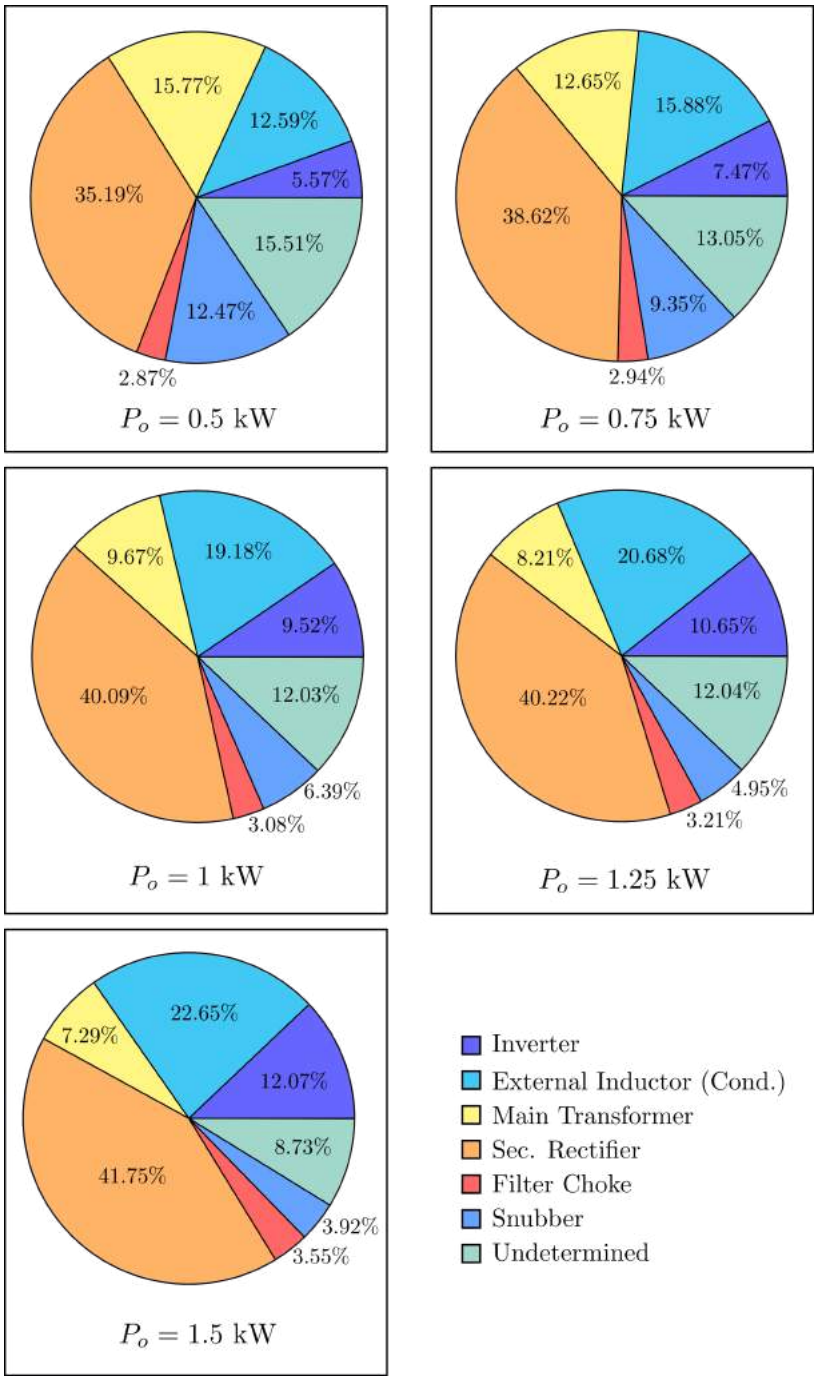


Fig. 5.21: Loss distribution (%) between different converter components.

snubber diode bridge are independent of the loading. The difference between the measured and calculated loss is termed as Undetermined in the pie charts.

5.6 Summary

This chapter covered the estimation of various parasitics using Frequency Response Analysis and through WE method utilising measured state variables. The experimental results proved the effectiveness of the proposed snubber in damping the secondary voltage overshoots. Further the laboratory experiments validated the converter design through experimental and analytical comparsion of the duty ratios. The converter can produce the required gain and achieve ZVS turn ON for all operating conditions. The analytical waveforms using closed-loop expressions derived in Chapter 2 matched the experimental waveforms of the converter establishing the accuracy of the PSFB analysis carried out in Chapter 2.
The loss distribution was implemented using the DFT on the measured converter currents and extracted parameters from the datasheet. It can be observed that the rectifier bridge and the series inductor account for around 60% of the total loss in the converter. The peak efficiency of the converter was measured to be about 92.95 at an output power of 0.75 kW%.

Chapter6

Conclusion and Future Work

A PSFB converter is a popular topology for medium to high-power electronics applications. Thanks to its simple phase shift modulation scheme that utilizes the converter parasitics to achieve ZVS turn ON. However, it suffers from a major drawback of voltage overshoots across the rectifier bridge. The existing solutions can be broadly classified into passive and active snubbers. Passive snubbers are easy to design and control but are lossy. The existing regenerative snubbers comprise active devices that require additional gate drive circuitry and increase the complexity of design and control.

6.1 Conclusion

The motivation of the thesis is to develop a snubber to overcome the drawbacks of the existing snubbers. The work introduces a novel snubber comprised of passive devices, thus overcoming the need for additional gate-driving circuits. Because the snubber doesn't include resistive components to dampen the voltage overshoots, theoretically making, it a lossless snubber.

Operational Analysis and Converter Design

The thesis presents a detailed analysis of the PSFB operation with the proposed snubber, considering all the major parasitics of the converter, like leakage and magnetizing inductances of the isolation transformers and device junction capacitances. The converter operation is divided into eight modes with clearly defined transition conditions. The analysis leads to the derivation of the closed-form expressions for the converter state variables. Using the converter gain and ZVS conditions obtained through the converter analysis, the thesis lays out a detailed design procedure for the PSFB converter. The design chooses suitable values for the leakage inductance L; the transformer turns ratio n and dead time. These parameters are selected so that all the inverter switches are soft-switched, and the PSFB achieves the specified voltage with the converter operating in the input voltage range of 360-440 V and the output power of 0.5-1.5 kW.

Experimental Validation

A 400/48 V, 1.5 kW hardware prototype with a switching frequency of 100 kHz is built to verify the operation of the snubber, analysis and the design of the converter. The analytical and experimental results show a significant reduction in the diode bridge voltage overshoots. The experimentally measured state variables clearly show all modes of operations. A close match of the analytical and experimental time intervals and the close

resemblance of the two waveforms confirms the accuracy of the analysis. The analytically predicted duty ratio matches the open loop duty required to achieve $V_o = 48$ V. Also, all the duty ratios are within the specified limits of d_{max} and d_{min}, confirming the proper design choice of n and L. The experimental results also validate the two ZVS conditions-availability of sufficient magnetic energy in the leakage inductance and proper dead time selection at $V_{dc,max}$ and $P_{o,min}$.

6.2 Observations and Future Work

Based on the observations of this work, the following things can be explored and further the research.

- The external inductor put to facilitate the soft-switching incurs 22% of the total loss at the rated load. Therefore, the inductor needs a significant design improvement to reduce these conduction losses.
- The secondary diode bridge sees 44% percent of the total loss at the rated load. The bridge can be replaced by synchronous rectifier to improve the effciency of the converter.
- The assumption of snubber circuit transferring 25% of the rated power leads to higher current rated diodes and larger snubber transformer. Thus, increasing the core losses in the snubber transformer. Therfore, an improvement in the snubber design is required. This could be improved assuming the snubber transfers 5-10% of the rated power.
- The ripple in the output current leads to a faster fall of the snubber current reducing the snubber conduction losses. Thus, the ripple in the output filter inductor can be incorporated in the anaysis and design of the converter.
- The parasitic capacitances are some of the important parameters in the design of the converter. Therefore, estimation of these parasitics is required to be explored to improve the accuracy of the design.
- The external inductor and the snubber circuit adds to the additional components which affect the size and efficiency of the converter. Therefore, a solution to integrate the magnetics must be explored.

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