Real-time AC Transmission Line Emulation with Power Electronic Converters

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Abstract—Advanced real-time power system analysis and testing demands accurate replication of the actual power system network in a lab-scale test-bed. Development of a programmable AC transmission line emulator becomes necessary for setting up such a representative power system network. Replacing a transmission line with an emulator involves - solving the exact transmission line model in real-time and controlling the emulator to follow the solved model. We present here a method of implementing the emulator using power electronic converters. Moreover, a numerical scheme for solving a distributed parameter long transmission line in an embedded platform has also been presented. Finally, relevant simulation and experimental results have been shown that validate the proposed emulation scheme.

Keywords—Telegrapher's Equation, Numerical solution, Current control, 3-phase VSI, back-to-back converters, real-time control, hardware emulation

I. Introduction

In the 1990s, the advancement of microprocessors and parallel computing concepts ushered in a new trend in power system analysis and testing with the invention of the Real-Time Digital Simulator (RTDS). It was then possible to thoroughly test the embedded control unit and protective relays employed in various power system applications, in a virtual environment before proceeding to real world tests of the actual system. This undoubtedly increased reliability, safety and enhanced quality of operation. This method, known as 'Hardware-in-Loop' (HIL) testing, was later extended to develop a real-time simulation environment capable of exchanging not only the low-level control signals, but also the power required by the Hardware under Test (HUT), such as-power converters, generators, PV inverters, motor, PV loads etc, [1]. For this purpose, power amplifiers are inserted between HUTs rated for higher power and the low-level simulator I/Os' (Fig. 1).

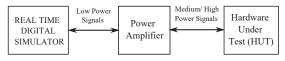


Fig. 1: A general block diagram of PHIL Testing.

However, despite all these advantages, the power system model in PHIL testing, is a simulated one which lacks practicality and PHIL suffers from accuracy and stability issues [2], [3] in closed loop operation due to imperfection of the power amplifier interface and computation time of the simulator. This makes the operation difficult and proper choice of

interfacing algorithms between the digitally simulated network and the HUT becomes necessary [4]. Due to these reasons, a more flexible and practical way to test equipments, control units and study power flow in large networks would be to replace the power amplifier based simulated system model with programmable hardware emulators (of each subsystem) that support real power flow in the network and mimic the real grid system operation with suitably scaled power and voltage levels, but with the same time constants as the actual system.

Transmission lines are central to the power flow in a large network or among networks. A transmission line emulator is therefore required to connect two buses physically present at any distance and study the power flow between them in various situations of interest. In this work, the development of such a flexible and programmable transmission line emulator has been addressed. The developed emulator can also function as a versatile test-bed for testing and studying synchronous generators, PV inverters, various loads etc. Due to flexible control modes and fast transient operation, the main building block of the proposed emulator is power electronic converters. In [5], similar problem of power converter based transmission line emulation has been addressed and two approaches towards the solution respectively in phasor-domain and time-domain have been proposed. The stability issues and some design considerations of this emulation have been studied in [6]. However, the scope of emulation in [5], [6] is limited only to short lines that too in steady state operation. Due to the lumped nature of the considered line and adopted implementation method, the above emulation fails to give accurate results in case of high frequency transients and longer transmission lines. In order to take care of these shortcomings, in this work, we propose and implement a Transmission Line Emulator (TLE), based on an architecture shown in Fig. 2 which can be used to emulate AC lines of any practical length, parameters and power level in both steady state and transient operation.

In the proposed architecture (Fig. 2), a suitably scaled down version of the transmission line terminal voltages is fed to the emulator. The emulator system senses these two voltages and passes the information to the Observer. The Observer running on a digital platform takes the two terminal voltage information as input, solves the actual transmission line mathematical model and gives the two terminal current information as outputs. This output information, which is a scaled down version of the actual transmission line terminal currents, is then treated as the reference and the power hardware output currents are controlled to follow that reference thereby, emulating the

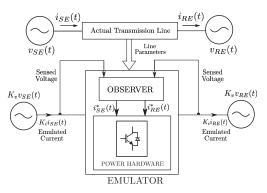


Fig. 2: The basic design of the Transmission Line Emulator (TLE).

actual transmission line in real-time in a scaled down fashion.

The approach used to solve a general transmission line in real-time using the Observer and its embedded implementation have been discussed in Section II. The emulation principle, different implementation aspects and proposed power converter topology are discussed in section III. Section IV talks about implementation of current control in case of a Grid-tied inverter used for line emulation purpose. Finally, simulation and experimental results of real-time emulation of a 3-phase transmission line have been presented in Section V. Section VI concludes the work.

II. REAL-TIME OBSERVER DEVELOPMENT

As a part of the overall TLE system (Fig. 2), the Real-time Transmission Line Observer performs the job of observing the emulated transmission line and predicting its terminal behaviour during various real-time events of interest. It does so by monitoring the Sending End(S.E) and Receiving End(R.E) terminal voltages and solving the S.E and R.E line currents based on the monitored voltage data. For the Observer to do this work accurately and robustly, it has to solve the transmission line mathematical model irrespective of any simplifying assumption regarding the nature of the line (long, medium or short) and the type of operation (steady-state or transient). For this reason, in this study, it has been decided to emulate a general uniform and lossy transmission line with frequency independent, distributed parameters so that, any simplification can be easily fitted into the model later, if necessary.

A. Modelling & Numerical Solution of AC Lines

Based on Fig. 3, the problem statement for the Observer can be formulated as: Given, a) Initial condition of voltages

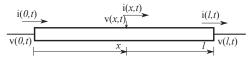


Fig. 3: Voltage(v(x,t)) and current(i(x,t)) at a distance x on a transmission line of length l.

and currents along the line: v(x,0) & i(x,0), and b) Boundary condition of voltages at both terminals: v(0,t) & v(l,t), solve the terminal currents: i(0,t) & i(l,t). To approach this problem, we start with the most general model of a transmission

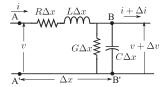


Fig. 4: Elemental section of a long Transmission Line.

line, an elemental section of which is shown in Fig. 4. The fundamental governing equations of voltage and current at a distance x from the sending end of a transmission line can be given as,

$$\frac{\partial v(x,t)}{\partial x} + L \frac{\partial i(x,t)}{\partial t} + Ri(x,t) = 0 \tag{1}$$

$$\frac{\partial v(x,t)}{\partial x} + L \frac{\partial i(x,t)}{\partial t} + Ri(x,t) = 0$$

$$\frac{\partial i(x,t)}{\partial x} + C \frac{\partial v(x,t)}{\partial t} + Gv(x,t) = 0$$
(2)

where R, L, G, C have their usual meaning. Substituting (1) into (2), forms a hyperbolic PDE known as the Telegraphers' Equation. Since, we are going to implement the Observer in real-time, we would focus on solving the above set of equations for i(x,t) and v(x,t) in the time-domain. However, obtaining the solution in frequency-domain is much easier, but, the transformed equations can be converted back into the time-domain only in special cases [7], when- a) Line is loss-less, or, b) Line is in sinusoidal steady state. No closed form analytical time-domain solution could be obtained for a practical line with losses and transients, and hence we need to rely on numerical methods.

The numerical method adopted in this work is known as 'Method of Characteristics' (MOC), a popular technique available in literature [8], used for solving hyperbolic PDEs'. The MOC converts (1) and (2) into ordinary differential equations that can be solved by integration only along a predefined family of lines which are known as characteristic lines (Fig. 5). In our case, these characteristic lines follow, $\frac{dx}{dt} = \pm \frac{1}{\sqrt{LC}} = \pm c$, where c is the wave propagation velocity along the transmission line. The physical significance of the characteristic lines is that a disturbance occurring at any point (x,t) in space and time on a transmission line, can travel both in the forward and backward directions along the line. The disturbance travelling in the forward direction follows the +ve characteristic line $(\frac{dx}{dt} = +c)$, while the disturbance travelling backward follows the -ve characteristic line $(\frac{dx}{dt} = -c)$. A solution for current and voltage can be obtained only at points in the x-t plane where the +ve and -ve characteristic lines intersect or where there is a single characteristic line and a boundary condition present (Fig. 5).

B. Embedded Implementation of the Observer

To apply MOC, the transmission line is divided into equal subsections of Δx starting from S.E (x=0) upto R.E(x=l)as shown in Fig. 5. These length steps are indexed by i, such that $x = i\Delta x$. So, i = 0 indexes S.E quantities and i = n indexes R.E quantities. The continuous terminal voltages $V_{S.E}(t)$ & $V_{R.E}(t)$ is sensed by the ADCs and sampled as discrete time signals, $V_{S.E}[k]$ & $V_{R.E}[k]$ with a sampling period T. These sampled values are fed to the Observer at

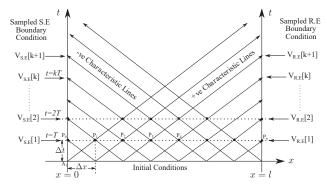


Fig. 5: Scheme for Digital Implementation of the Observer.

every $[k]^{th}$ computation time step as boundary conditions. The Observer then solves the line equations and gives the $[k]^{th}$ step S.E and R.E currents, $I_{S.E}[k] \& I_{R.E}[k]$, which are used as reference for the subsequent current control loops. The $[k]^{th}$ step solved values are again used to solve the $[k+1]^{th}$ step values in the next computation cycle and in this way the numerical scheme advances in real-time. Therefore, for stable operation, it becomes a mandatory requirement to keep the Observer computation time $(t_{comp,obs})$ less than the sampling period T.

The discretized solution for currents and voltages on a transmission line obtained after application of MOC in our case, is given in difference equation form in equations (3)-(7). At the k^{th} time step, (3) gives the S.E current, (4) and (5) gives the voltage and current respectively at the i^{th} point $(1 \le i \le n-1)$ on the line and (6)-(7) gives the R.E current and R.E voltage respectively considering a resistive termination.

$$I_{S.E}[k] = C_1 V_{S.E}[k] - C_2 V_1[k-1] + C_3 I_1[k-1]$$

$$V_i[k] = C_4 \left(V_{i-1}[k-1] + V_{i+1}[k-1] \right)$$

$$(3)$$

$$+ C_5 \left(I_{i-1}[k-1] - I_{i+1}[k-1] \right)$$
 (4)

$$I_i[k] = C_6 (V_{i-1}[k-1] - V_{i+1}[k-1])$$

$$+ C_7 (I_{i-1}[k-1] + I_{i+1}[k-1])$$
 (5)

$$I_{R.E}[k] = C_8 V_{n-1}[k-1] + C_9 I_{n-1}[k-1]$$
(6)

$$V_{R.E}[k] = R_L I_{R.E}[k] \tag{7}$$

 $C_1,...,C_9$ are constants for a particular line whose values are given in the Appendix. The discussed numerical scheme was coded in Matlab/Simulink and transmission line equations were solved. The steady state and transient behaviour of the developed solution were then compared against two available transmission line models in PSCAD software, namely- the Bergeron model and the Frequency Dependent Phase Model (latest and most accurate) (Fig. 6). In all cases, the line was terminated with a resistance, $R_L = 300\Omega$. The line parameters were, length (l) = 100 kms, L = 2.16 mH/km, C = 7.512 nF/km, $R = 0.1052\Omega$ /km, $G = 1.05 \times 10^{-8}$ mho/km.

III. CONVERTER TOPOLOGY & IMPLEMENTATION

A. Converter Topology

Conceptually, the essence of transmission line emulation using power electronic converters is to control the output line currents of two back-to-back Voltage Source Inverters (VSI)

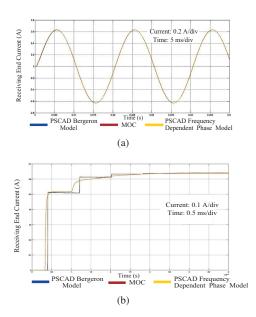


Fig. 6: Comparison of developed numerical scheme with standard PSCAD models: (a) The steady state R.E current due to sinusoidal excitation of 230V at input, (b) The transient R.E current due to step excitation of 230V at input.

in such a way that they can behave like an AC transmission line at a scaled down power and voltage level (Fig. 7). The back-to-back VSIs' are grid-tied on both sides, where the grid voltages are an appropriately scaled down version of the actual transmission line S.E and R.E terminal voltages with the S.E voltage leading the R.E voltage by a phase angle δ .

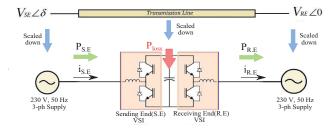


Fig. 7: Actual Transmission line replaced by scaled down Emulator.

The emulator is developed for mimicking the transmission line behaviour in broadly 3 situations- a) Steady-state, b) Electromechanical transients and c) Electromagnetic transients. However, in this work only the steady state and low frequency transients emulation have been addressed. We will focus on the power electronic hardware and associated control mainly targeted for steady state transmission line emulation. For steady state (50 Hz) and electro-mechanical oscillations (0.1-3 Hz), balanced system operation can be assumed and the typical frequencies in the line current to be tracked is in the order of 50 Hz. So, converters with switching frequencies within 10 kHz can be used.

B. Scaling of the actual system

The system initially considered in the problem consists of a 250 km, 3 phase transmission line carrying power between

two buses at 22 kV having a power angle difference δ . The transmission line parameters and voltage and power base of the actual system are tabulated in Table-I. For the purpose of emulating the transmission line using laboratory-scale power electronic hardware, we need to scale down the system from the actual power level (10 MVA) to the power level of the 3-ph VSIs used for emulation (15 kVA). To preserve system equivalence, this scaling has to be done keeping the per unit values of power, voltage and line characteristic impedance same. However, to get proper transient performance, no scaling needs to be performed in time-domain since the wave propagation characteristics remain unaltered in the scaled emulator system. Doing such we get the following table-

	TABLE I: Scaling of parameters.
ntity	In Actual Transmission Line

Quantity	In Actual Transmission Line	In Emulator
Power Base	10 MVA	15 kVA
Voltage Base (L-L)	22 kV	400 V
Line Parameters		
Length	250 km	250 km
L	0.63 mH/km	0.139 mH/km
С	9.4 nF/km	42.6 nF/km
R	19.5 mΩ/km	4.264 mΩ/km
G	1.05×10 ⁻⁸ mho/km	

C. Emulation of Transmission Line Losses

Practically, in order to achieve a low-cost solution for the development of the emulator system we intend to develop the system with a single DC source that will provide the DC bus to both the S.E and R.E VSIs'. In this emulator topology (Fig. 7), as we replicate the transmission line currents at both ends, the VSI used in the sending end takes up power equal to sending end power $(P_{S.E} = V_S I_S)$ of the transmission line and gives it to the DC bus, from which the receiving end power ($P_{R.E}$ = V_RI_R) as needed by the receiving end VSI is supplied. But since the emulated transmission line is lossy, the power lost in the line resistance, P_{loss} ($P_{loss} = P_{S.E} - P_{R.E}$) is the net power that should be taken up by the DC bus (Fig. 7). Commercially available DC sources generally do not support reverse power flow and this excess power (P_{loss}) is taken up by the DC bus capacitor. To prevent this, we need to put a DC source that supports reverse power flow and control the DC bus voltage. This issue has been taken care of by employing an Active Front-End Rectifier (AFE) to do active rectification of the available 3-phase mains voltage and by controlling the output DC voltage of the AFE using conventional inner current and outer voltage loop control method. Alternatively, a single phase Boost PFC (Power Factor Correction) rectifier can also be used.

Based on the considerations as discussed above the proposed transmission line emulator system topology is as shown in Fig. 8. In Fig. 8, the two VSIs' (in red) used for emulating the S.E and the R.E of a transmission line have been interfaced with similar grid emulators (in blue) on both ends. A grid emulator on one side can be replaced by a synchronous machine for testing purposes. The AFE (in black) supports the loss power and holds the DC bus voltage steady.

IV. CONTROL IMPLEMENTATION

Based the proposed Transmission Line Emulator (TLE) concept, the two grid-tied VSIs' used for emulating the sending

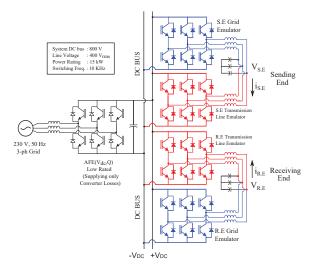


Fig. 8: Proposed topology of the Transmission Line Emulator test-bed.

and receiving end of a transmission line have been controlled in current control mode in order to track the Observer generated current references. The controllers have been designed in the rotating dq0 frame so that the reference currents appears as DC and can be tracked using simple PI controllers. The VSIs' are synchronized with the grid voltages using Synchronous Reference Frame - Phase Locked Loop (SRF-PLL).

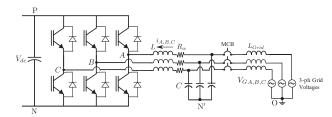


Fig. 9: A 3-phase Grid-Tied VSI emulating one end of a transmission line.

The controlled grid-tied VSI system has been shown in Fig. 9, where, the filter inductor currents, $i_{A,B,C}$ are controlled. Using the grid voltage phase angle information from the SRF-PLL, this system is transformed from the A,B,C frame to the rotating dq0 frame. The SRF-PLL aligns the d-axis of the rotating frame with the d-component of L-N grid voltage vector, $\vec{V_g}$ ($\vec{V_g} = V_{gd} + jV_{gq}$) such that, $V_{gq} = 0$. In Fig. 10, the d-axis current control block diagram is shown. In this block diagram we consider, $P(s) = \frac{1}{sL + R_{\alpha}}$ as the plant, the inverter output voltage (V_d) as the plant input and the grid voltage (V_{gd}) as external disturbance. G_{inv} represents the average model of the VSI. Since the plant, P(s) to be controlled is a first order system and the reference signal is DC, a PI controller, $C(s) = \frac{K_{PI}}{s} \left(1 + \frac{s}{\omega_{PI}} \right)$, is sufficient to eliminate steady state error. The controller design has been done by cancelling the plant pole $(\frac{R_{\alpha}}{L})$ by the PI controller zero (ω_{PI}) and then tuning the gain \vec{K}_{PI} to get desired openloop bandwidth. The open-loop BW should be kept less than or equal to $\frac{1}{10}$ th of the switching frequency. In our case, the BW is kept around 400 Hz. Feed-forward of the grid voltage

disturbance (V_{gd}) and the q-axis current cross-coupling term (ωLI_q) is necessary to fully cancel their effects. The detailed implementation of the control loop is shown in Fig. 11 in block diagram form. The controller gives the inverter voltage reference (v_d^*) , which is frame transformed into ABC frame and the divided by the DC Bus voltage (V_{dc}) to get the modulation signal (d_{α}^*) . Common mode (d_{cm}) is then added and the obtained duty signal (d_A^*) is scaled up by the carrier gain (V_M) and sent to the FPGA for comparison and PWM pulse generation.

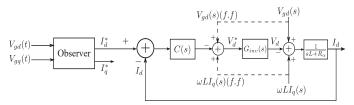


Fig. 10: The d-axis current control loop. The q-axis current control loop is similar to the d-axis.

The DSP and FPGA platform used in this work is based on $Zynq\ All\ Programmable\ SoC$ (System on Chip) made by Xilinx. For CSV-PWM signal generation, the carrier was implemented in the FPGA part of $Zynq\ SoC$, and dual-edge duty cycle update method was used. This dual-edge sampling (at every $0.5T_{sw}$) of the duty period in a single carrier cycle (T_{sw}) results in relatively better inductor current waveform than single-edge sampling.

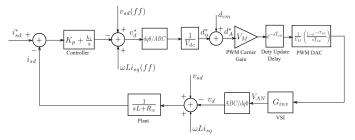


Fig. 11: Block diagram of detailed implementation of the current control loops.

V. SIMULATION & EXPERIMENTAL RESULTS

To verify the emulation scheme, a scaled-down Transmission Line Emulator (TLE) prototype is designed and fabricated, as shown in Fig. 13. The system parameters are summarized in Table II. In the present case, only the S.E of the emulated line is connected to the grid, the R.E of the line is connected to a resistive terminal load (R_L) of 100 ohms (Fig. 12). Similarly, the R.E can also be connected to the grid and power flow between two areas can be studied. The same controls will be applicable in that case as well.

TABLE II: System Parameters

Parameter	Value
S.E Grid voltage	120 V(L-N)
DC Bus voltage	400 V
Line inductance	6 mH
Switching frequency	10 kHz

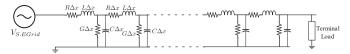


Fig. 12: A distributed parameter, lossy transmission line with terminal load taken up for emulation. The line parameters are given in Table-I.

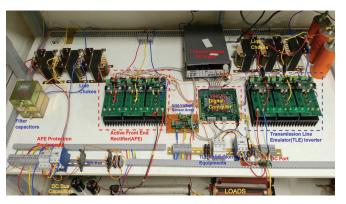


Fig. 13: Experimental Set-up of the TLE system.

A. Steady state operation with steady S.E Grid voltage

In the first experiment, the S.E grid voltage of the TLE was kept fixed at 120 V_{L-N} . This is actually 52.2% of the base voltage of the TLE (Table-I). This 0.522 p.u voltage translates to 6.63 kV when scaled up to the actual transmission level. The steady-state S.E line current magnitude and phase, as drawn by the TLE in experiment are verified against PSCAD simulations (Fig. 14-15). It can be seen in Fig. 14(b), the S.E voltage (blue) fed to the TLE and the S.E current (pink) drawn by TLE is identical with the simulation (Fig. 14(a)). Fig. 15 shows a comparison between simulation and experimental emulation for verifying phase angle difference in steady state. For the actual line in PSCAD, the phase difference between the phase-A S.E voltage (yellow) and phase-A S.E current (blue) is 31.5° lagging. TLE generated phase-A S.E current (pink) lags the applied phase-A S.E grid voltage (blue) by 30.96°. The phase difference closely matches for other phases as well.

B. Transient performance with swelling grid voltage

The low frequency transient (1-10 Hz) performance of the emulator was verified by linearly increasing the S.E grid voltage over 5 line cycles and comparing the S.E current drawn by the emulator with that drawn by an actual transmission line in PSCAD simulation. Result shown in Fig. 16. The S.E current (pink) behaves exactly like the actual case (Fig. 16(a)) when S.E grid voltage (red) is changed from 30 V (0.13 pu) to 120 V (0.52 pu).

VI. CONCLUSION

The work presented in this paper had successfully met two major goals - power electronic converter based programmable AC Transmission Line Emulator prototype development and implementation of the controls that make the developed prototype a 'flexible' Transmission Line Emulator. The developed emulation scheme is independent of the transmission line type and can be equally applied for emulation of high frequency

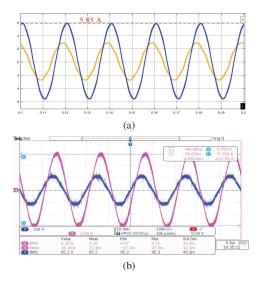


Fig. 14: Comparison of simulation and experimental emulation for steady state operation: (a) PSCAD simulation of Sending End (S.E) phase-A voltage (yellow) & current (blue) of an actual transmission line. [Scale: X-axis: 10 ms/div; Y-axis: 80V/div(voltage), 2 A/div(current)]; (b) Real-time emulation.

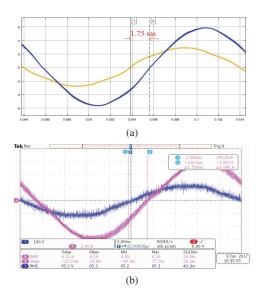


Fig. 15: Phase angle verification: (a) PSCAD simulation. [Scale: X-axis: 10 ms/div; Y-axis: 80V/div(voltage), 2 A/div(current)]; (b) Real-time emulation.

transients. In the scope of the work, experiments of real-time AC transmission line emulation in case of steady state and low frequency transient, have been successfully conducted and the experimental results have been validated against simulations. The future work will be the emulation of symmetrical and asymmetrical line faults using the developed prototype.

APPENDIX LINE CONSTANTS

The constants $C_1,...,C_9$ used for solving a transmission line with parameters R,L,G,C,R_L in eqns. (3)-(7) are given as follows- $C_1=\frac{A}{B},C_2=\frac{A'}{B},C_3=\frac{B'}{B},C_4=\frac{0.5A'}{A},C_5=\frac{0.5B'}{A},C_6=\frac{0.5A'}{B},C_7=\frac{0.5B'}{B},C_8=\frac{A'}{AR_L+B},C_9=\frac{B'}{AR_L+B}$

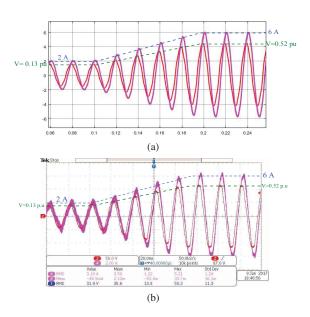


Fig. 16: Comparison of simulation and experimental emulation in case of varying grid voltage: (a) Simulation of S.E current (pink) behaviour due to swell in S.E grid voltage (red). Scale: X-axis: 20 ms/div; Y-axis: 75 V/div (voltage), 2 A/div (current); (b) Real-time emulation of part (a).

where,
$$A = \left[\sqrt{LC} + \frac{G}{2}\sqrt{\frac{L}{C}}T\right]; B = \left[L + \frac{RT}{2}\right]; A' = \left[\sqrt{LC} - \frac{G}{2}\sqrt{\frac{L}{C}}T\right]; B' = \left[L - \frac{RT}{2}\right]. T \text{ is the sampling time.}$$

ACKNOWLEDGMENT

The authors are grateful to the Department of Science & Technology (DST), Govt. of India, for approving the "Fund for Improvement of S&T Infrastructure" (FIST) Program at the Dept. of Electrical Engineering, IISc Bangalore that has supported the project financially.

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